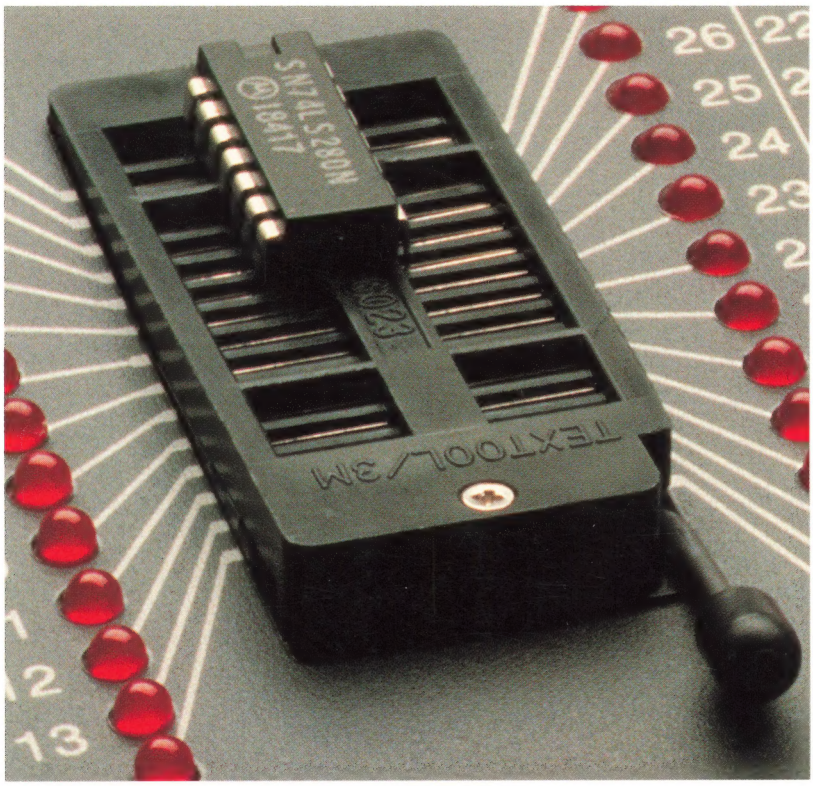
# 900 SERIES • SOLUTIONS

## DYNAMIC TROUBLESHOOTING




Self-Paced Tutorial

FLUKE®

# Fluke 900
## Dynamic Troubleshooter

Self-Paced Training

FLUKE

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Revision 1.0


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# SECTION 1
## Introduction

## 1 Introduction and Basic Concepts

Congratulations on your purchase of a Fluke 900 Dynamic Troubleshooter. This self-study guide will provide you with all the basics needed to successfully apply the 900.

- If you are a technical manager or a user of pre-programmed Test Sequences, you will become familiar with the essential techniques of Dynamic Troubleshooting after completing Section 1 and 2.
- If you are a technical specialist who will be developing Sequences, you will want to review this entire Self-Paced Training guide as a foundation for further reading in the Operator Manual.

Section 2 covers all the testing features of the machine and its application to various devices. It can be completed in 2 hours. The instructions are sequential and it is recommended that they be completed from start to finish, in order.

Section 3 is a short tutorial on storing a Test Sequence to the Cartridge. It may be supplemented with the Getting Started tutorial documented in the 900 PC Software Operator Instructions for those interested in Sequence creation on a PC.

Section 4 consists of a series of exercises that explain and illustrate each test parameter. This section may be completed in any order, though it is recommended that each exercise be completed in order.

Section 5 describes the procedure for adding a new device to the tester's Standard Library. This is the library that uses Reference Devices (RDs). Simulation Libraries which do not need RDs cannot be developed by the user and are added at the factory under the ongoing Library Maintenance Program.

If you have trouble with any part of this course, in the USA call 1-800-53FLUKE for assistance from a technical specialist. Outside the USA contact your local Fluke Sales Representative, or call (206) 347-6100 and ask for Manufacturing R&D, Board Test Support.

Other relevant documentation includes the 900 Operator Manual and the 900 PC Software Operating Instructions. They provide a complete reference of the tester and software operating features. Appendix I of the Operator Manual is entitled Applications and it has advice on testing a variety of device types. Look here also for application advice

listed by specific device number.

This course had been designed to accompany two different training boards. The two possible boards are a PC-XT style Personal Computer system board with separate power supply (self-paced trainer), and a PC-XT style Personal Computer system board mounted on a white plastic frame with power supply on the underside (sales demo trainer).

Accompanying this course book you will find two additional manuals, a TTL Databook, and a booklet titled Microprocessor Solutions. The databook is provided because many technicians do not have such data readily available to them, and it is very useful when troubleshooting with the 900. The Microprocessor Solutions booklet is a condensed primer on microprocessor type circuit boards. It can be read as a refresher in under half an hour, or it can be studied by someone new to microprocessor technology as a guide to future reading.

It is recommended that anyone preparing to use this self-paced tutorial first review the Microprocessor Solutions booklet. When troubleshooting with the 900 it is often as important to understand signal flow through a board as it is to understand how an individual device truth table is applied to the actual device.

# 2 Description of the 900

The Fluke 900 is a benchtop test system used to isolate faulty digital devices on electronic circuit boards. It requires the board being tested to be powered and operating (to the extent that it exhibits a board level fault.) One way of thinking of this is that the 900 is used in the same environment in which troubleshooting with an oscilloscope is performed. By clipping over an entire IC and evaluating its functionality at speed in its operating environment, it is a much more powerful approach than using conventional instruments. Its ability to store Test Sequences on a removable cartridge puts automated troubleshooting procedures in the hands of a less experienced operator.

The standard configuration of the 900 comes complete with the items and accessories listed below. Please take a moment to check that they are available for use with this course.

900 Dynamic Troubleshooter, includes:

- 900 Main Unit
- Interface Buffer

Three Test Clips:

- 16-pin, 0.3" Test Clip (Y900-16D)
- 24-pin, 0.3" Test Clip (Y900-24D)
- 28-pin, 0.6" Test Clip (Y900-28D)

- 32 Kbyte Data Cartridge (Y900-001)
- Set of 5 Patch Cords (Y900-005)
- RD Tray & Cartridge Holder (Y900-003)
- User's Manual

Training Kit, includes:

- PC-XT style computer system board
- Daughter board PCB (installed in math co-processor socket of system board)
- PC-XT style Power Supply
- Reference Device chipset
- Fault insertion clip lead
- Data Cartridge with course material stored in it
- TTL Device Data Book
- Microprocessor Solutions Book
- (This training course book)

Device Simulation is now included as a standard feature to minimize the handling of Reference Devices, and make troubleshooting more convenient. It supports in- and out-of-circuit testing of TTL devices and compatible technologies (i.e. 5 volt supplied ROMs, RAMs, PALs, etc.). Also supported by Simulation is out-of-circuit testing of 14XXX/ 4XXX series CMOS devices, which may have supply voltages up to 15 volts.

There is an unadvertised option for the 900 that is rarely recommended because of certain restrictions that it places on in-circuit testing. This option, the 900-002 CMOS Option, is for certain specific applications where the additional capability to test and identify this technology out-of-circuit is required. That is, CMOS devices may be inserted in the ZIF socket for out-of-circuit verification or identification. This option does not enhance the in-circuit comparison testing of CMOS devices, though it reduces the maximum data rates testable from 20 MHz to 16 MHz for all devices.

Additional clips that may be ordered cover the range of DIP packages from 8 to 28 pins, the range of SOIC Surface Mount packages from 8 to 28 pins, and PLC devices in 20 and 28 pin square packages. The PLC clips come standard with a square PLC adapter for conversion to the DIP socket on the 900. A 16 pin High Impedance Clip is available that minimizes the in-circuit loading effect of clipping on low drive capability components (i.e. CMOS).

Extra Data Cartridges may be ordered in 32 Kbyte and 64 Kbyte sizes for storing Test Sequences and data files.

For order information, see the Technical Data brochure on the Fluke 900 Dynamic Troubleshooter (in the USA call 1-800-44FLUKE), or contact your local Fluke Sales Representative.

The Library Utility is a set of PC diskettes that contain Library Files of the latest devices supported by the 900 and a file management utility for downloading them to the tester. The Library Utility is updated periodically. Updates for the first year are included[①] with new system purchases.

The 900 PC Software package (900-903) is an option used to develop Test Sequences in a friendly PC environment. Downloaded Sequences may be executed from a stand-alone 900 or under full control of a PC. The main benefits of the package come from using the PC's full screen display, tactile keyboard and disk storage capabilities. Or, if you prefer to include the 900 with an existing custom test station, you may choose to implement the 900 Remote Control commands in your application software (see Appendix III of the 900 Operator Manual for remote control command set.)

([①] Updates to the Simulation Library will be sent to the address indicated on your *900 Registration Card* at no charge for the first year. If the *Registration Card* is not returned, we will use the shipping address where the 900 was originally sent. Be sure to indicate the name of the actual user of the 900 on the card. We have found that without the mailing address of where the 900 is actually used, and name of user, the updates often fail to reach the same. If you have not received any updates within six months, call 1-800-53FLUKE in the USA, or write to John Fluke Mfg. Co., Inc., 900 Product Manager, Mail Stop 246F, PO Box 9090, Everett WA 98206, to correct the mailing address and user name in our database. Requests or suggestions of chips that you would like to see included in the next library release may be directed to the same address or phone number. Contact your Fluke Sales Representative about a 900-901 Library Maintenance Agreement Renewal to continue receiving updates after the first year.)

# 3 Where to use the 900 Tester

## Functional Test Fault Isolation

The 900 is used to isolate faults on boards that are failing a functional test. That is, a board is powered and activated and it exhibits a failure at the board level. Testing may be done in a hot mock-up, a final system, a stand-alone micro-based board, on a board stimulated through a microprocessor emulator pod, or stimulated by some other test system. The 900 may be used anywhere you may now be using an oscilloscope to trace faulty digital signals.

The 900 monitors activity without affecting the board under test. It isolates faulty devices in their circuit without artificially backdriving devices like in-circuit testers. In this way, testing is performed under natural operating conditions and speeds. This permits a high quality of test and fault capture.

## Test vs. Diagnosis

The basis of Dynamic Reference Comparison is to use, as the diagnostic stimulus, the functional go/nogo test that confirms a board is failing. A question sometimes asked is: "How complete a test does the 900 do?". The answer is: as complete a test as the stimulus that exercised the fault. Some features of the 900 such as Activity Check and display of the number of RAM locations written during a test, can indicate how complete a stimulus is. In general, however, if a board is failing, the fault is being exercised and the 900 will capture it.

# 4 900 Terminology

New terms used in this course are:

**Reference Device (RD)** A replacement IC that is used as a hardware model for comparison. The RD is placed in the ZIF socket where it is subjected to a copy of the signals measured on the Device Under Test (DUT). If the RD responds differently than the DUT, a failure is recorded.

**Device Under Test (DUT)** The IC located on the Unit Under Test (UUT) that is suspected as failing.

**Unit Under Test (UUT)** The target board that is exhibiting a failure. This board must be powered and active, though the activity may be severely limited by failures.

**Performance Envelope (PE)** Working in conjunction, two test parameters (Threshold and Fault Mask), define the optimum timing characteristics for a comparison test of any individual signal transition.

**Main Unit** The part of the 900 that has the keyboard and display.

**Interface Buffer** The rectangular pod with two ribbon cable connectors, J1 and J2, used to plug IC test clips into. It translates voltage levels on a board into 900 internal levels. (See warning in Section 2, part 1.)

**Patch Leads** The 5 removable black leads that insert into the Interface Buffer and attach to nodes of a test board. GND, EXT, RST, VCC labels mean Ground (GND should be used at all times), External Input, Reset, and Vcc (Vcc is used exclusively with Reset, and is not required in most cases).

**ZIF Socket** The Zero Insertion Force (ZIF) socket on the Main Unit that accepts a Reference Device (RD).

**Monitor LEDs** The LEDs around the ZIF socket that display logic status of the RD pins. Also, a failing pin LED remains flashing after a failure is captured.

**Size LEDs** The horizontal row of LEDs located above and to the right of the ZIF socket that identify the column of numbers that apply to pins of a specific Reference Device.

**Cartridge** A black plastic pack containing either 32 Kbytes or 64 Kbytes of nonvolatile memory storage that inserts into the right side of the Main Unit.

**RD Tray** A convenient antistatic foam retainer for Reference Devices and Cartridges. One tray per board type is recommended.

# SECTION 2
## 900 Operation

## 1 Testing With the 900

Ensure that you have all the materials for the training course as described in Section 1.

To prepare the Fluke 900 for use, first make sure that the Interface Buffer is plugged into the Main Unit through connectors J1 and J2. They are labelled and keyed, and are not interchangeable.

| | |
|---|---|
| **WARNING:** | Connectors J1 and J2 must never be connected or disconnected while the Fluke 900 power is on. If they are connected or disconnected while power is applied, the Interface Buffer ***will*** be damaged, and the 900 mainframe ***may*** be damaged. |

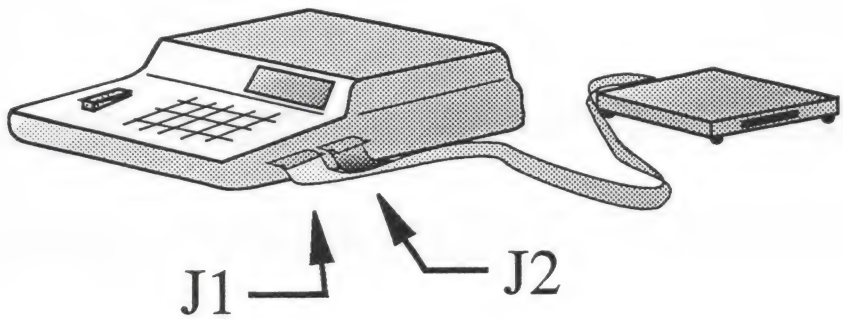



Figure 1

It is possible to operate the 900 mainframe without the Interface Buffer being connected, some limited operations may be performed. When the Interface Buffer is completely detached, the 900 will fail selftest, but will not be damaged. If the Interface Buffer is connected, then ***both*** connectors J1 and J2 must remain properly attached at ***any time*** that the power is applied.

To turn the unit on after connecting the Interface Buffer and AC power cord, press the toggle switch located on left side toward the rear. You should observe the following:

- There will be a brief hesitation before any activity begins.
- Green power LED illuminates.
- The LCD screen reads "Memory Test". The memory test is the first of over 50 hardware tests.

- After approximately a minute of Selftest there is an audible tone, and the main menu screen appears.

There are six common situations that will result in an apparent selftest failure. Any of the six situations listed below will cause the selftest to fail, but does no damage to the 900 or the device.

- A Reference Device is inserted in the RD ZIF socket of the 900 mainframe.
- A Test Clip from Interface Buffer is clipped over a device on the board under test.
- The EXT Patch Lead from the Interface Buffer is attached to the board under test.
- A keyswitch is depressed either on the 900 mainframe, or the Interface Buffer.
- A Y900-16DZ High Impedance Test Clip was attached to the Interface Buffer.
- The Interface Buffer is completely disconnected from the 900 mainframe (see warning described in figure 1).

A Selftest failure appears as follows:

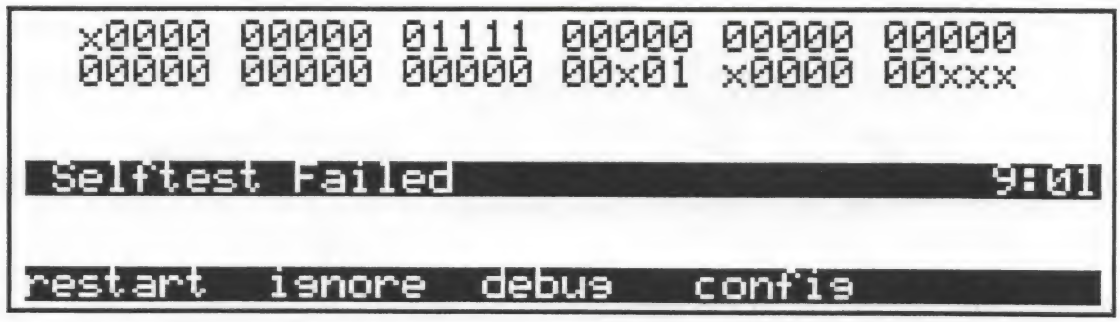



Figure 2

The function keys of the 900 always correspond to a set of key labels printed directly above them on the Liquid Crystal Display (LCD). In this instance, the key label "ignore" corresponds to the function key F2 on the keyboard. Pressing F2 (ignore) will allow you to proceed with keyboard and file operations, but will not permit actual DUT comparison testing.

You may re-run the Selftest again by pressing F1 (restart). A true Selftest failure is diagnosed from the rows of 1s, 0s, and Xs displayed on the screen which represent the hardware test failure number and failing channels. If a true hardware fault is suspected, press F3 to enter debug mode. A printer may now be connected to the serial port (See Section 1.6.2 in the Operator Manual for serial port settings). Select soft menu key F3 (prt_res) to print out a diagnostic listing. This printed listing will greatly assist authorized service personnel in determining the exact problem.

Upon successful completion of Selftest, the main screen appears as follows:

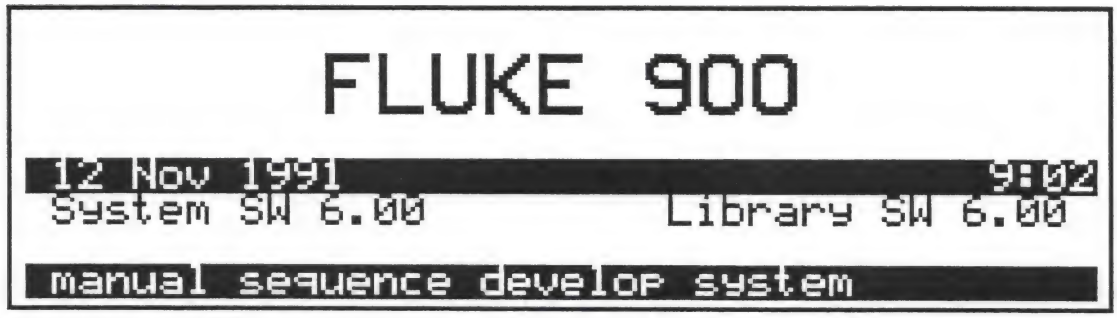



Figure 3

The highlighted line in the middle of the screen is referred to as the Status Line. The Status Line in the above screen shows the date and time. User feedback, various indicators, and range limits of some parameters will appear on this line as appropriate.

The firmware revision level of the machine is found above the function key labels that are on the bottom line. System Software refers to the ROM-based operating system of the tester. Library SW refers to the ROM-based library of devices supported within the tester. In some units there may be two ROM libraries present, sales demonstration units are an example. A standard library designated X.XX (e.g. 6.00) supports devices that are testable using physical Reference Devices. The Library Utility Software package is used to create user library files and send them to the tester/cartridge. The downloaded libraries will contain standard library information, and may also contain device simulation or RAM shadow information, depending on the device and how the Library Utility has been configured.

Notice the function keys (F1) through (F5) and the labels above them on the screen. The labels change according to a menu tree. You will find a quick reference guide at the back of this course book. Two other keys are found with the function keys:

(ESC) returns control to a previous menu level.
(ETC) displays more labels available on a current menu level.

The alphanumeric keys are used for data entry and are upper case by default, (press shift to obtain lower case.)

(CE) (Clear Entry) performs a backspace function to delete the last character.
(SHIFT)(CE) deletes the last word entered.
(CNTR)(CE) deletes the last line entered.

(ENTER) terminates a line of data. As you will see, it typically puts user inputs into the fields of the main display.

(TEST) and (NEXT) are found on the right side of the keyboard. These keys are used for test execution, and to step from device to device when executing a preprogrammed test Sequence.

The function keys on the main level represent the four major modes of the tester:

(F1) manual
To use as an instrument in manual or immediate mode. You may select a component and modify test parameters as necessary when default values are not suitable for the current test. Out-of-circuit testing is normally done in this mode.

(F2) sequence
To execute stored Test Sequences and operate the unit like an Automatic Test System. Permanent alteration of the stored Test Sequence is not possible in this mode.

(F3) develop
To create or modify Test Sequences and perform file management tasks.

(F4) system
To configure system options: time and date, sound, RS232 port, printer format, service debug.

Develop Mode is sometimes preferred over Manual Mode. Note that all test capabilities available in Manual Mode are available from Develop Mode. The advantage offered by Develop Mode is that any test created in Develop Mode may be stored for later use. This avoids having to re-discover or re-enter the appropriate parameters for a specific device later, and will greatly accelerate creation of Test Sequences for all of your workload. Even if only a small percentage of a given board is tested during any single session, the next time that board type is tested those locations will already be pre-defined and available. With this incremental approach, manual testing from Develop Mode will quickly result in a completed Test Sequence for a board. The only drawback to developing test sequences in this manner on a failed board, is that there will necessarily be a lower confidence in the resulting test parameters until they have been verified on a good board.

# 2 Out-of-Circuit Testing

*In this section you will test devices in the Reference Device Socket, verify a PAL and a standard 74xx series device, and match an unidentified chip with its generic equivalent number. You will gain some familiarity with Manual Mode operation of the 900. To gain familiarity with the menu structure of the 900 more quickly, locate the Menu Tree listing in the back of this course book. Trace your menu selections through the tree as you complete each exercise.*

## 2.1 Creating a PAL Checksum Test

**Exercise**

Press [F1] (manual) to bring up the following screen. Note the operator prompt "Enter selection or chip name" seen just under the Status Line of the display.


Figure 4

The upper left corner of the screen is used to display device numbers. It is now blank, and all displayed test parameters are set to system default values.

Load the device library description for a Programmable Logic Device of the type PAL22V10, press [P], [A], [L], [2], [2], [V], [1], [0], [ENTER].

Press [ETC] to show additional menu labels, and press [F3] (rd) to choose the Reference Device (RD) functions of the tester. Notice that the programming equations of the PAL, and resulting checksum are unknown to the tester.

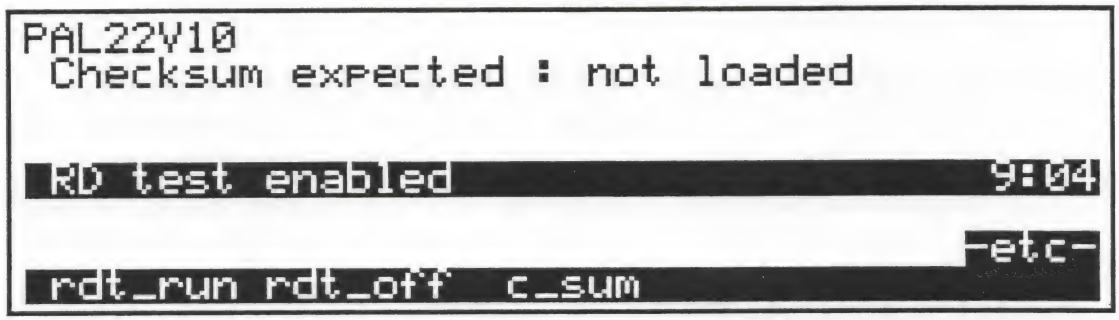



Figure 5

Remove the reference devices from their static protection, and insert them in the black anti-static foam of the RD Tray in the back of your Operator Manual. Then take the PAL22V10 from the RD Tray (it has been programmed and labeled DEMO3), and place it in the Zero Insertion Force (ZIF) socket of the tester with pin 1 of the device lined up to pin 1 of the socket. Lock the device into the socket by pulling the locking lever forward and down.

Press F1 (rdt_run) to run a standard Reference Device Test. Note that the test fails. When testing a custom or programmable device, the 900 expects a "checksum". Since this is the first time we have tested this device in manual mode, the checksum is not known. We can calculate and store this checksum, and verify that the checksum calculated produces a repeatable result.

Press F3 (c_sum) and type in the actual value found, followed by ENTER.

Re-run the RD Test, press F1 (rdt_run), to verify this checksum (i.e. the test now passes). A characteristic checksum may also be created for ROM and EPROM devices in a similar manner.

**Summary**

Because of the many opportunities for error in programming, labeling, and revision control for programmable devices, it is important to ensure that the device used for reference against a suspect DUT is the correct device. Checksum verification of the RD is a simple and effective method to ensure that comparison will be made using the correct RD. Checksums may be calculated quickly and easily by the 900 despite limited knowledge of the RD.

## 2.2 Standard Device Testing

*Testing of common TTL and CMOS devices may be done using the RD truth tables in the standard library. The desired device must first be selected at the Manual level.*

**Exercise 1**

Press [ESC] after the previous exercise to return back up to the "Manual" level. Note that the operator prompt "Enter selection or chip name" seen at the beginning of the previous exercise is not present at this time. Although the prompt is not displayed after first entering Manual Mode, it is possible to load a new library definition any time you are at this level of the menu.

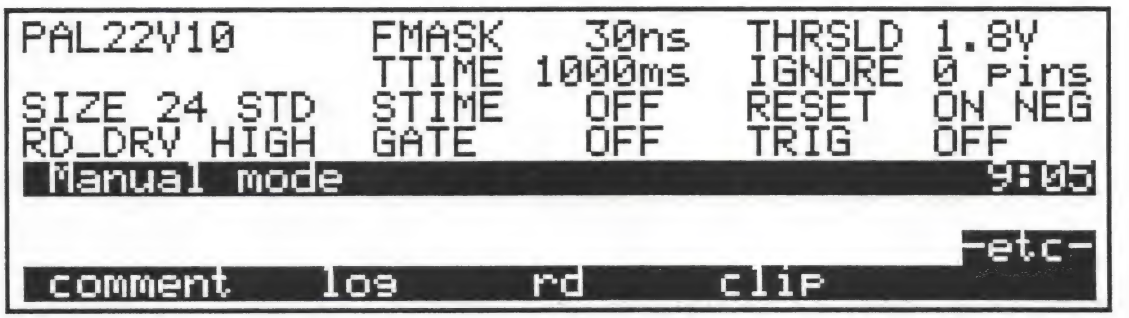



Figure 6

Load the device library description for a 7474, press [7], [4], [7], [4], [ENTER].

Note that the logic family designator 'LS' of the RD was not included in the name. As long as there are no differences in the truth table of the device between different logic families (S, LS, ALS, F, etc.), the family designator is not included in the library name for devices. See Appendix IV of the Operator Manual for a full list of available library definitions, and the name by which they are known to the library.

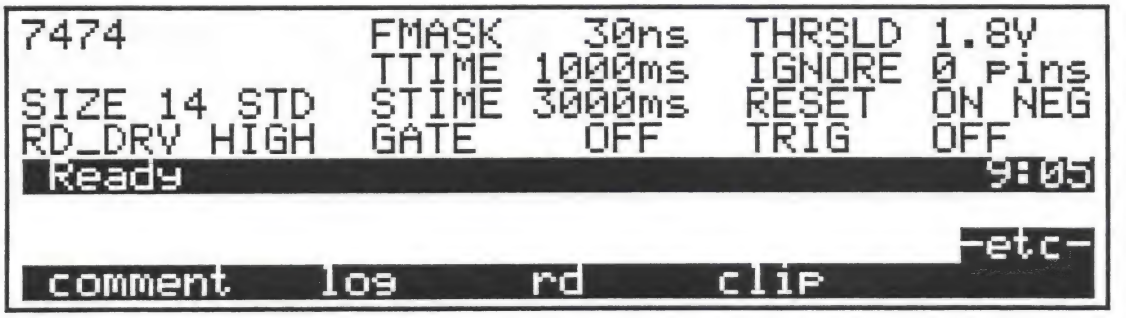



Figure 7

Insert a 7474 device into the ZIF socket (device pin 1 lined up with socket pin 1), and run an out-of-circuit test on the 7474 by pressing [F1] (rdt_run).

The out-of-circuit device test reads a vector table from the ROM Library, and applies it to the device in the ZIF socket. If, according to the vector truth-table, the RD responds correctly, it will receive a Pass test result. This test is done at approximately 10 KHz. Because of the slow speed of the test, this out-of-circuit test should not be thought of as thorough test of the RD.

**Exercise 2**

Locate the Training Data Cartridge that was provided with this course. Insert the cartridge firmly into the slot on the right side of the tester. Re-load the device library description for the 7474 by typing [7], [4], [7], [4], [ENTER].

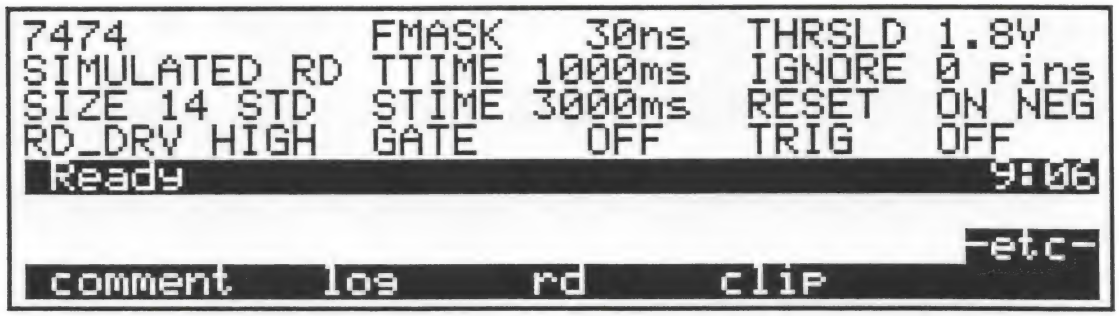



Figure 8

As shown above, if a Simulation Library for the selected device is resident in the tester you will observe the message SIMULATED RD on the second line of the display. The Simulation Library may have been downloaded to either System RAM or a Data Cartridge, or installed as a special Demo ROM Library. If one of the above sources is not available the menu selection will not be displayed, and a physical RD will be required. If the word 'simulation' is displayed, a high-speed re-programmable gate array chip inside the tester has been configured to perform the same logical function as the physical RD, and thus no physical RD is required. Simulation may be used in place of physical devices for applications up to about 16 MHz data rates, depending on the complexity of the device being simulated. For faster applications, a physical RD is recommended.

Press [F3] (rd) to obtain the screen shown in figure 9.

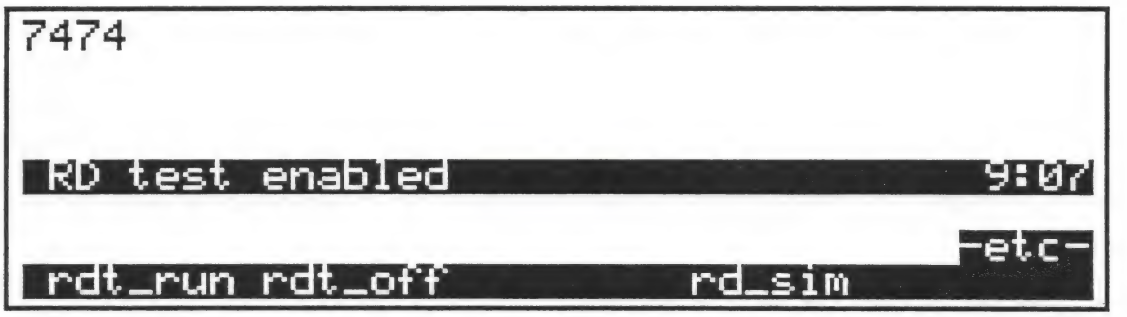



Figure 9

You may disable the simulation feature by pressing F4 (rd_sim), F1 (on/off), ENTER. Notice that on the Menu Tree, many selections are in *italics*. If a particular selection is not always present, it will be displayed in italics on the Menu Tree.

Whether or not Simulation is enabled, or even present, a physical device is always required in the ZIF socket for the F1 (rdt_run) selection. At all other levels of the menu tree, a Simulated device will be used if selected.

## 2.3 Identifying an Unknown Device

*Manufacturers will often re-label common ICs to fit their needs. This situation presents troubleshooting problems for all technicians other than those working for that manufacturer. The 900 is able to use test vectors from the RD verification test to identify unlabeled or privately labeled ICs by comparing their logic functions to common IC types. If identification is successful, an industry standard IC could be used as a replacement.*

**Exercise**

Press (ETC) to display more menu labels.

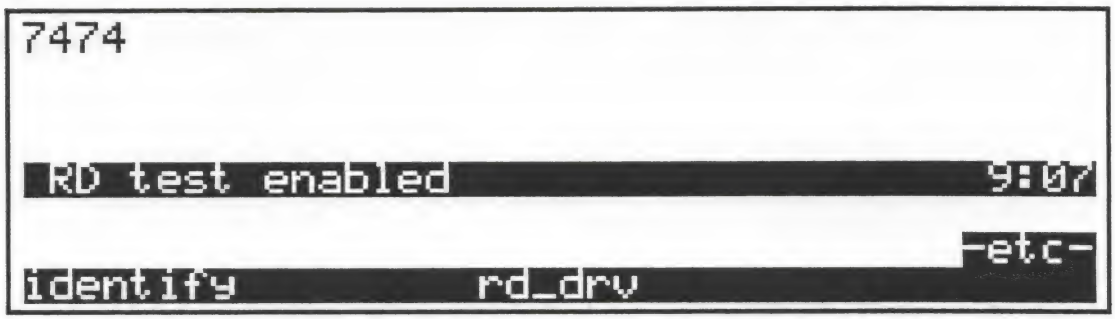



Figure 10

Insert any 74XX series device from the RD Tray into the ZIF socket and press (F1) (identify). Note that the current device size setting is still 14 from our previous test of a 7474.

Press (F1) (no) in response to the prompt "Identify according to selected size?," if the device you selected does not have 14 pins. Proceed to type in the correct size for the device you have inserted (e.g. 20 for a 74244), followed by (ENTER).

Pressing (F5) (yes) now will cause the tester to try and match the device in the ZIF socket with the 74XX patterns in its RD Test truth table library. The 900 will only check device descriptions for devices having the specified number of pins.

This selection will identify most known devices. A 'known' device is one described in a library resident in the tester's data cartridge, system memory, or ROM library at the time the selection is executed. It will identify most chips that fall into the category of Combinatorial or Synchronous as described later in this text. It will not identify any devices categorized as Programmable.

The rd_drv selection also displayed on this screen is used to alter the characteristics of the ZIF socket to permit testing of weak output devices. By changing the rd_drv setting

from high (default) to low, the current applied to the device in the socket is reduced to one-third of normal. Making this change allows some Static RAMs, some EPROMs, and many CMOS devices to be used in the RD socket. Try setting rd_drv to low when you have verified that a known good device is in the socket, but are still getting the message 'RD test failed ...'

Press [ESC] twice, and [F5] (yes) to exit back to the main screen.

**Summary**

The test parameters associated with Reference Devices are found in the RD menu option. Within this menu are features for out-of-circuit testing of 54/74XX series and 14/4XXX series devices, and checksum testing of ROM/EPROM and custom PAL devices. Unknown devices may be identified against the TTL standard library using the Identify feature. Control is found here for other RD parameters such as Simulation and RD Drive. When testing devices in their circuit, RD Test is used as a check that an operator has inserted the correct, functioning Reference Device if required. This check may be disabled and re-enabled using the rdt_off/rdt_on function key found on the RD menu.

# 3 In-Circuit Testing

*In this section you will cover the range of troubleshooting features offered by the 900 to test devices in their circuit and isolate faults on digital circuit boards. Three subsections illustrate the* ***primary*** *test results and how they are achieved for combinatorial, synchronous and programmable devices. The signal measurement capabilities of the* ***secondary*** *condition tests are described in a separate section. You will gain familiarity with the Sequence Mode of operation.*

## 3.1 Primary DRC Test

The primary test uses the technique of Dynamic Reference Comparison to compare a suspect device under test (DUT) with a known good Reference Device (RD). The RD may be an actual device, or one that is simulated in hardware by the 900's re-programmable gate array. The stimulus pattern is the full speed natural activity of the board; the board is often referred to as the unit under test (UUT).

The routing of signals from the DUT through the tester is shown in the diagram in figure 11. The inputs measured at the DUT are recreated as input signals to the RD. Since the RD is powered up and operating, it responds to these input conditions and produces outputs. The outputs from the DUT are compared in real time against the outputs of the RD. A mis-match, at any time during the comparison test, indicates a failure.

The Diftest Circuit automatically determines which RD pins are inputs and which are outputs. This pin by pin evaluation of the RD is done in real-time, with no performance loss. In fact, other than the truth-table data provided for RD functional verification, there is no data supplied by the 900 Libraries to indicate pin direction (input or output). The exercise using the *size* parameter in Section 4 demonstrates a useful application of the Diftest circuitry.

In summary, the DRC technique analyzes the full functional performance of the DUT, operating in the circuit under test, by comparing its performance to the performance of a known-good reference device. The know-good device is either "simulated" by hardware in the tester or, if the tester cannot simulated the device (such as custom logic), a known-good replacement part for the suspect component can be inserted in a ZIF socket provided for this purpose on the front panel of the tester.

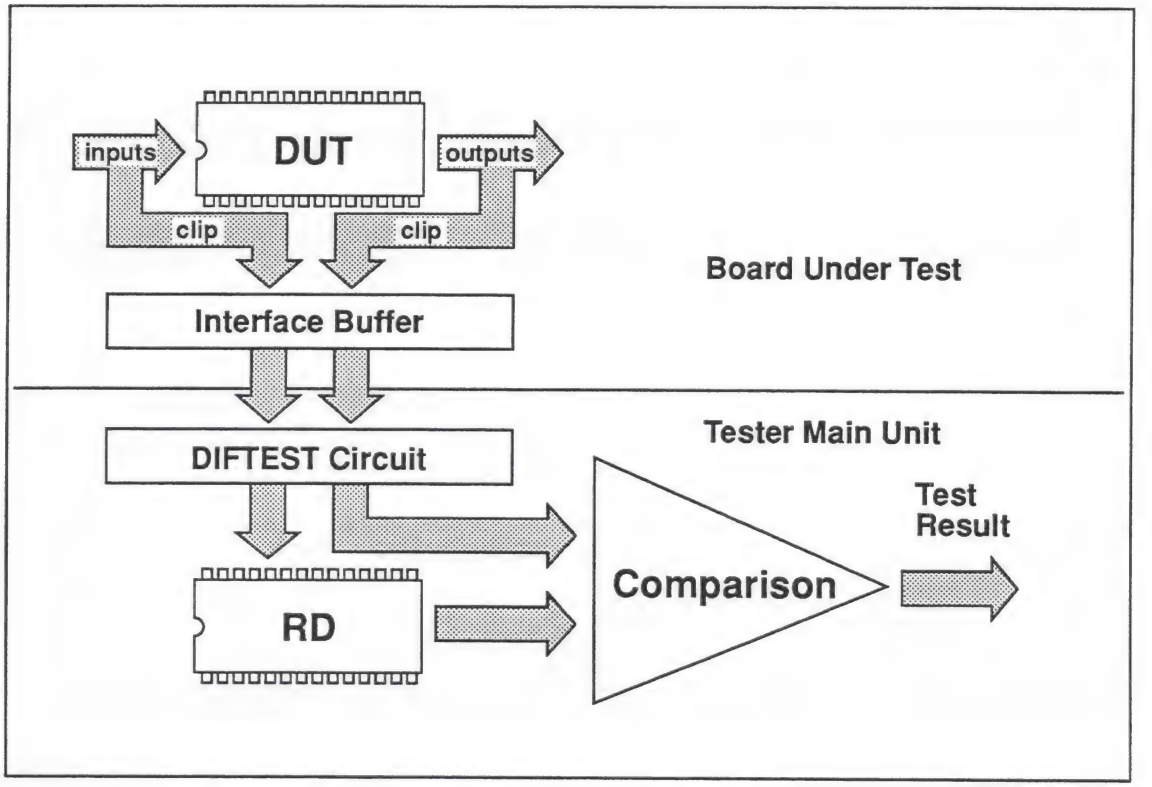



Figure 11

Ensure that the training data cartridge is inserted in the right side of the tester. From the main menu, select [F2] (sequence) to obtain the screen shown below:

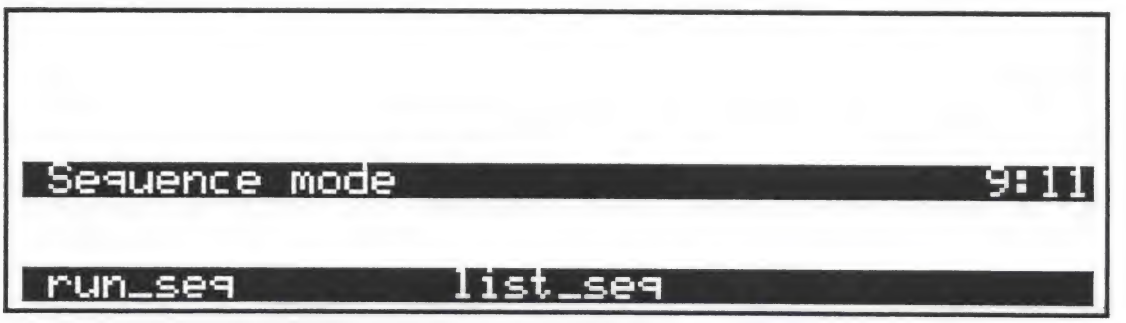



Figure 12

Press [F3] (list_seq) to observe a directory listing of the Sequences on the cartridge.

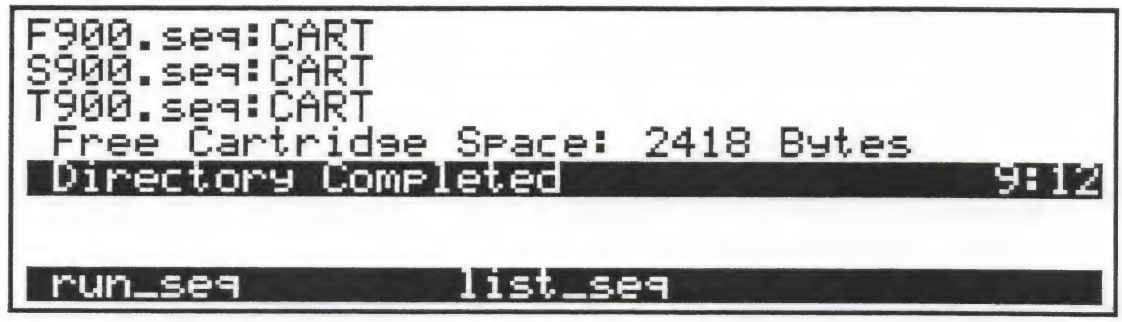



Figure 13

For the self-paced trainer, load the T900 training sequence, press [F1] (run_seq), [T], [9], [0], [0], [ENTER]. If you are using the sales demo trainer board, load the S900 training sequence instead. The first screen of the T900 Sequence is shown below:


Figure 14

This screen shows how messages can be embedded within the Sequence. Lines 2 through 4 of the screen were added as operator prompts. A Sequence is a preprogrammed troubleshooting procedure consisting of a series of ordered device tests, their associated test parameters and any desired operator prompts. Press [NEXT] to bring up the next screen of the test sequence.


Figure 15

Follow the operator prompt and connect up the Interface Buffer Patch Leads to posts for the Reset button connector as shown in the drawing in figure 16 of the self-paced trainer board. The tester will issue a reset pulse to the board to force execution of its power-on self test. Ensure that the UUT is connected to a power outlet and turned on. (On the sales demo trainer use the GND(Ground) and RST(Reset) posts located just over the power supply. You may need to press the red button switch on the board to activate the LEDs that indicate the board is operating).

The group of colored LED's is driven by a control line from the microprocessor, and should be active at all times.

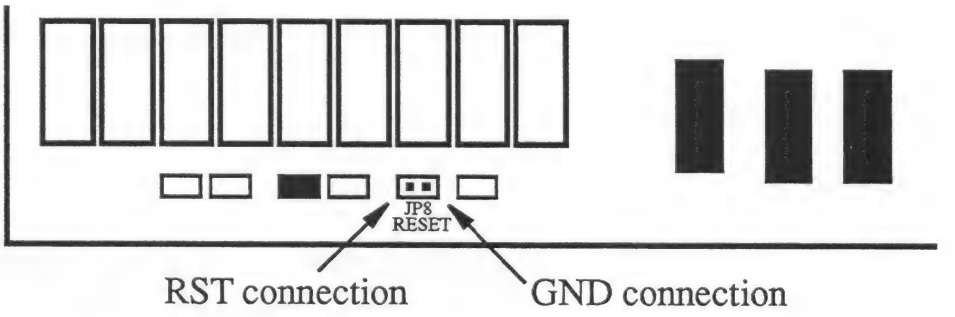



Figure 16

Press (NEXT) to bring up the first device test.

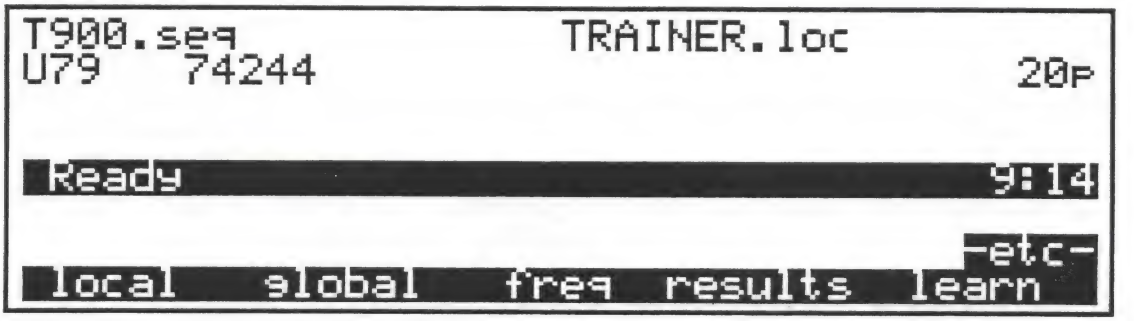



Figure 17

Select a 74244 Reference Device from the RD chipset and lock it into the ZIF socket.

Select the 24 pin Test Clip and insert it into the Interface Buffer. It is keyed and contains only passive components. Larger clips may be used successfully on smaller components as long as pin 1 (see label) is properly aligned, and the clip seats fully on the DUT – even if some pins from another device are also clipped.

Clip over U79 on the board, taking care to position pin 1 of the Test Clip over pin 1 of

the DUT (use U37 on the sales demo trainer).

Press [TEST]. You should obtain a PASS test result. If the RD is missing, reversed in the socket, or not aligned properly to pin 1 of the socket, the message "RD test failed ..." appears in the status line of the display. If the clip is reversed or offset so that pin 1 was not aligned properly to DUT pin 1, the message "Vcc-GND check failed" appears on the status line of the display. Both failures will have no ill effect on the RD or DUT, and you may reposition the RD or the clip and test again. Note that if you attempt to test a device and the UUT is not powered up, you will also receive the "Vcc-GND check failed" message.

After obtaining a PASS test result, press [F4] (results) to examine detailed test results for the preceding test. We will cover these in more detail in a later exercise.

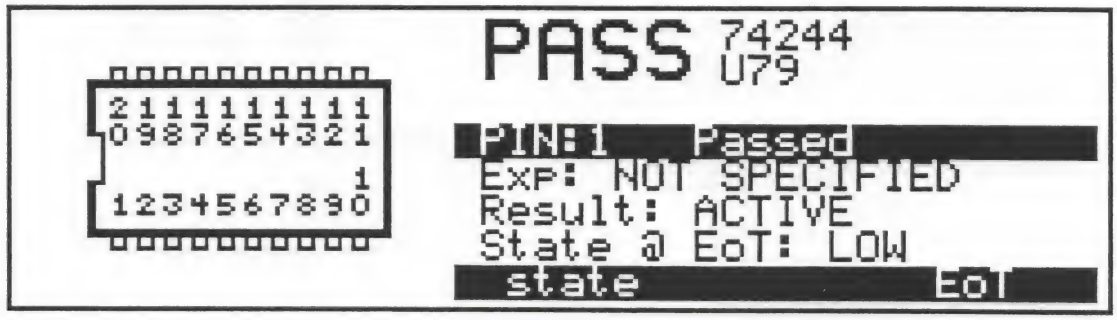



Figure 18

The flashing cursor can be moved with the four arrow keys to point to individual pins. This is used to examine the logic activity information that the 900 collects on all pins during a test. To see a "summary" of the activity on each pin during the preceding test you can press [F3] (state).

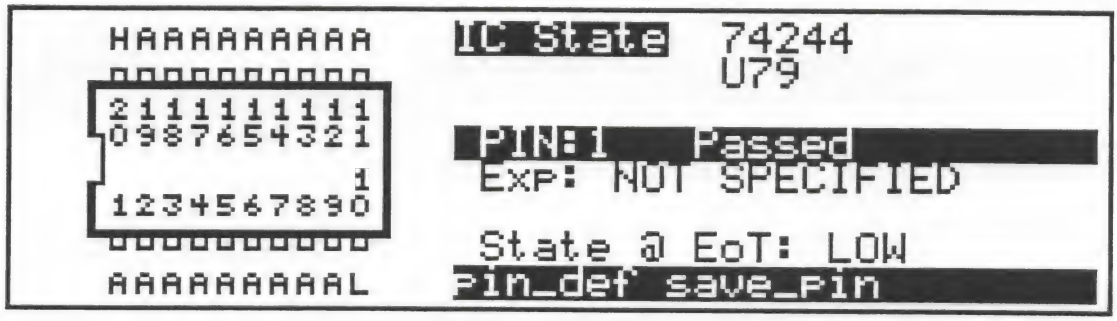



Figure 19

The symbol A means that the pin was active and made at least one transition during the preceding test. L means it was always Low, and H means it was always High.

Press [ESC] followed by [F5] (EoT) to see a "snapshot" of all pins at the End of Test (EoT).

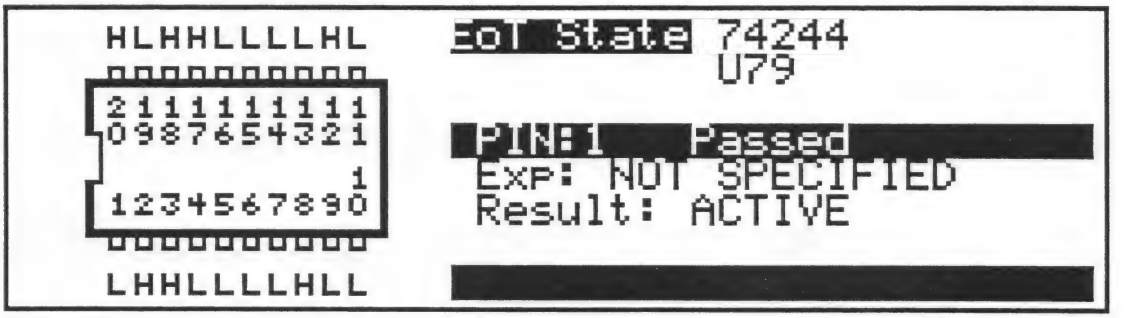



Figure 20

Any time during a test that a mis-match of outputs between the RD and DUT exceed the limits defined by the current test parameter settings, the test will be halted and test results will be available. At the specific instant that a test is stopped, the logic value of each pin is recorded. In the example above the test stopped because it ran for the full duration of the test time (t_time) parameter. Had a failure been detected, the test would have been halted immediately, and this screen would show the logic value measured on each pin at the instant of failure. From the EoT screen, a technician can decode the address, data, and control line information present on the DUT at the time of failure.

Press [ESC] twice to see the following screen:

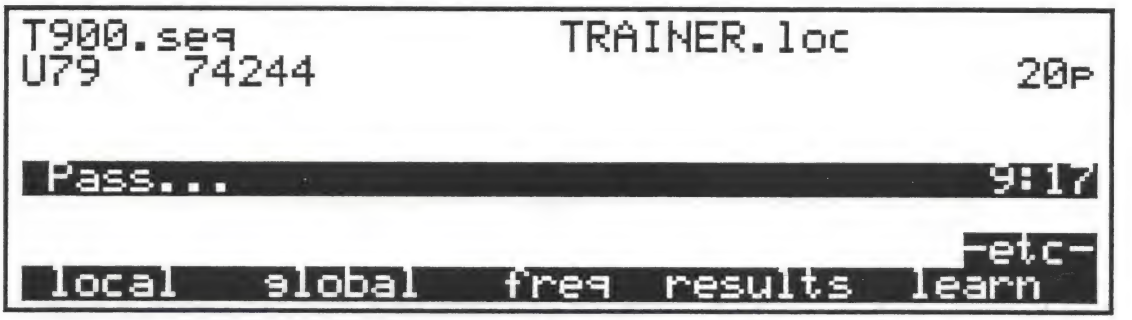



Figure 21

The menu option "local" refers to the test parameters for only this chip (U79), while "global" refers to the default parameters that apply to all the chips on the board. Press [F1] (local) to reveal the test parameters for U79.


Figure 22

In this exercise you will change the test parameter 't_time' (test time), to be continuous. It can be a useful thing to do when trying to find intermittent faults, since the DUT can be heated or cooled while testing, until a failure occurs. Press [F1] (t_time), [F2] (cont.), [ENTER] and observe how the value for Test Time has changed. Note that while t_time is selected, the status line displays the range limits for this parameter, (1 - 9999ms). Press [TEST] to initiate a continuous test and observe the activity monitor LEDs around the ZIF socket.

Locate the black fault insertion lead that was included with this training kit. It should have a female connector on both ends, and black shrink wrap over an axial leaded 2200pF capacitor in the center. Remove the clip ends from two Patch Leads and attach them to the fault insertion lead. Attach one end of the fault insertion lead to pin 14 of U80. Then while the test is running, momentarily touch the other end to pin 10 of U80. (If you have the sales demo trainer press the blue Fault Switch labeled F8. The red LED beside it should illuminate.)

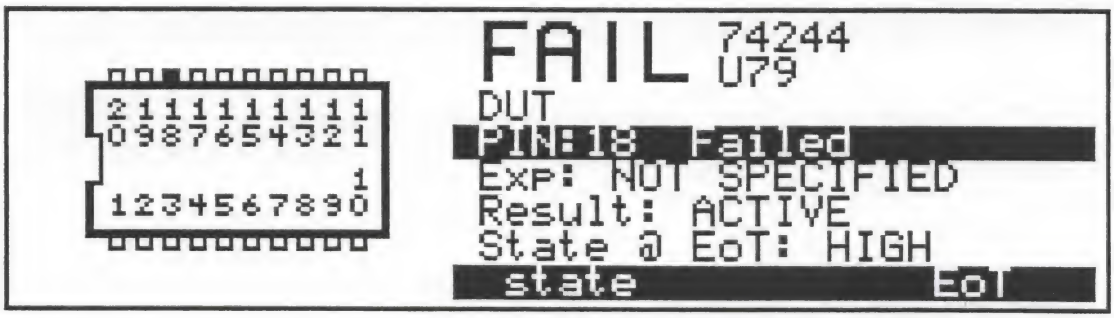



Figure 23

This faults the signal on pin 18 of U79 by putting a capacitive load on address line A0 to delay the rise and fall time of the signal (see the diagram in figure 24). The top signal is what was measured before the fault was inserted, the bottom signal was measured with the fault.

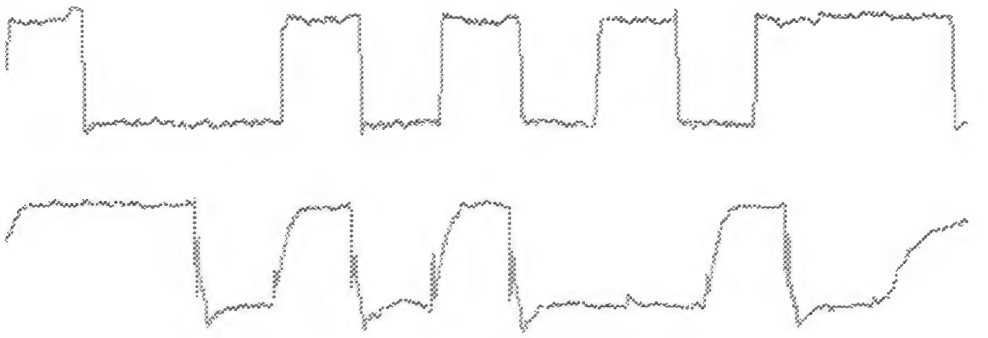


Figure 24

A comparison failure should have occurred. More detailed information on this failure is provided later (see figure 27). One of the LEDs around the ZIF socket should be blinking, and a second one right above the number 20 should be on constantly. Below the LED that is on constantly, find the pin number across from the blinking LED. You should find that pin 18 has failed. The LEDs around the ZIF socket are called the Monitor LEDs. Across the top of the number field are found the Size LEDs, which help identify pin numbers. After a failing test, the LED(s) corresponding to pin(s) that did not match the RD will be blinking, and the word "DUT" will be found directly beneath the FAIL message. If a test fails and no LEDs are blinking, then the failure was due to a secondary conditions test failure, and word "Conditions" will be found under the FAIL message. It is possible to fail both DUT and Conditions on multiple pins. More explanation about conditions testing is provided under Pin_Def in Section 4.

If you press [F3] (state) you will observe that pin 18 was active. This is typical of a dynamic timing fault.

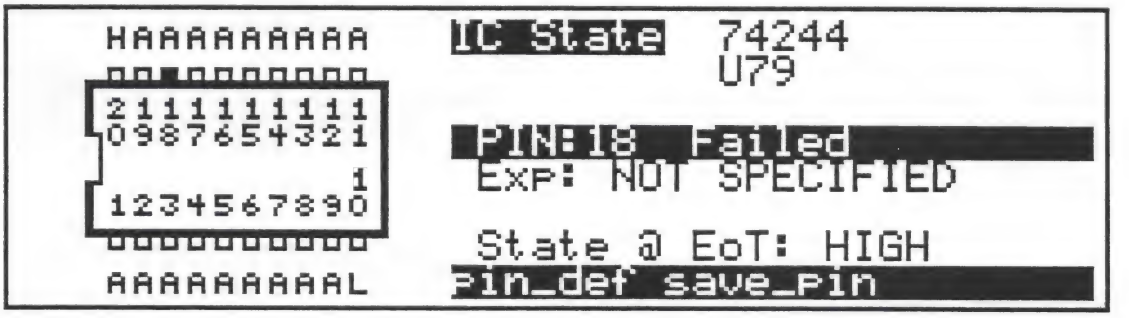



Figure 25

Press [ESC] three times to return to the U79 Sequence screen, and [NEXT] to bring up the next test in the Sequence. This is a duplicate of the last test, except that the RD is simulated. Remove the physical RD from the socket. The preceding tests and fault insertion can be repeated using a simulated Reference Device with equivalent results.

## 3.2 Testing Combinatorial Devices

*This subsection examines the testing parameters of the simplest devices: combinatorial ICs. The concept of a Performance Envelope (PE) is introduced to define a tolerance of the test. Tristate devices, combinatorial and otherwise, can have special requirements. A tristateable bus driver is provided as an example of a combinatorial device with special requirements.*

*A combinatorial device has outputs that are a function of its immediate inputs. There are no internal states or storage elements. Buffers and gates as well as tristateable drivers are examples of combinatorial devices.*

### 3.2.1 In-Circuit Loading on the DUT

Ensure that the display is showing the U79S Sequence screen of the last exercise (for the sales demo trainer it will be U37S). If you are elsewhere in the Sequence, simply type in (U), (7), (9), (S), (ENTER) when the status line reads "Ready", and the U79S screen will be loaded.

Re-insert the fault from the previous exercise. Attach one end of the fault insertion lead to pin 14 of U80, and the other end to pin 10 of U80. (If you have the sales demo trainer press the blue Fault Switch labeled F8, the red LED beside it should illuminate.)

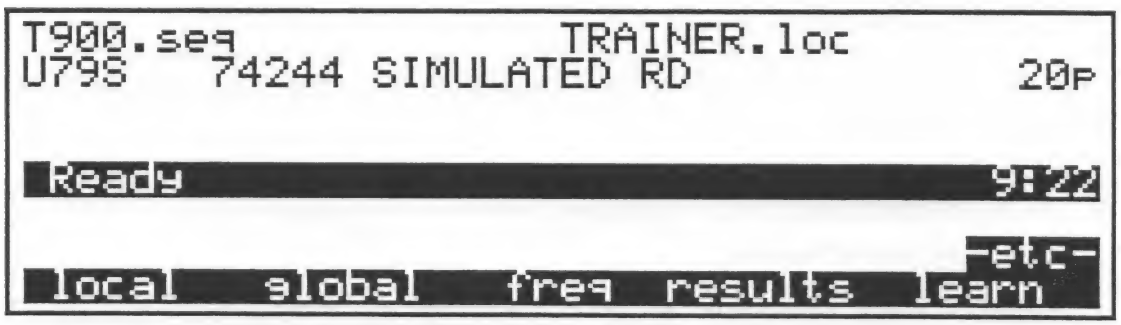



Figure 26

Press (TEST) and observe that the test now fails. Press (ESC) to leave the Fail screen, then experiment with higher values of F_Mask until you get a value that results in a Pass.

Press (F1) (local), and (F2) (f_mask) to change the Fault Mask parameter. Notice that while F_Mask is selected, the Status Line displays the range limits for this parameter. All values of F_Mask are set in 10 ns increments.

Type in a new value, such as (7), (0), then (ENTER).

To try the new value press (TEST).

Repeat this process until you have found the value of F_Mask that is just barely large enough to pass consistently. Verify that this setting is just large enough by trying the next smaller increment of F_Mask to get a failing test result.

Circle the smallest value of F_Mask that would still result in a Pass:

30 40 50 60 70 80 90 110 120 130 140 150 160 170 180

The Performance Envelope consists of the F_Mask and Threshold parameter settings (see figure 27). Fault Mask is the compensating parameter for timing differences between the RD and DUT. Refer to the diagram below. The DUT is subject to loading from the circuit it is driving, and the output signal will rise, fall, or both more slowly than the same output signal of the RD. F_Mask is used to establish a tolerance for the real-time comparison between signals of the DUT and RD. On a good board you can find the best setting of F_Mask by trying different values until a test passes consistently. F_Mask also compensates for differences in timing due to the technology of the DUT (LS, ALS, F, etc.) and the real or simulated Reference Device.

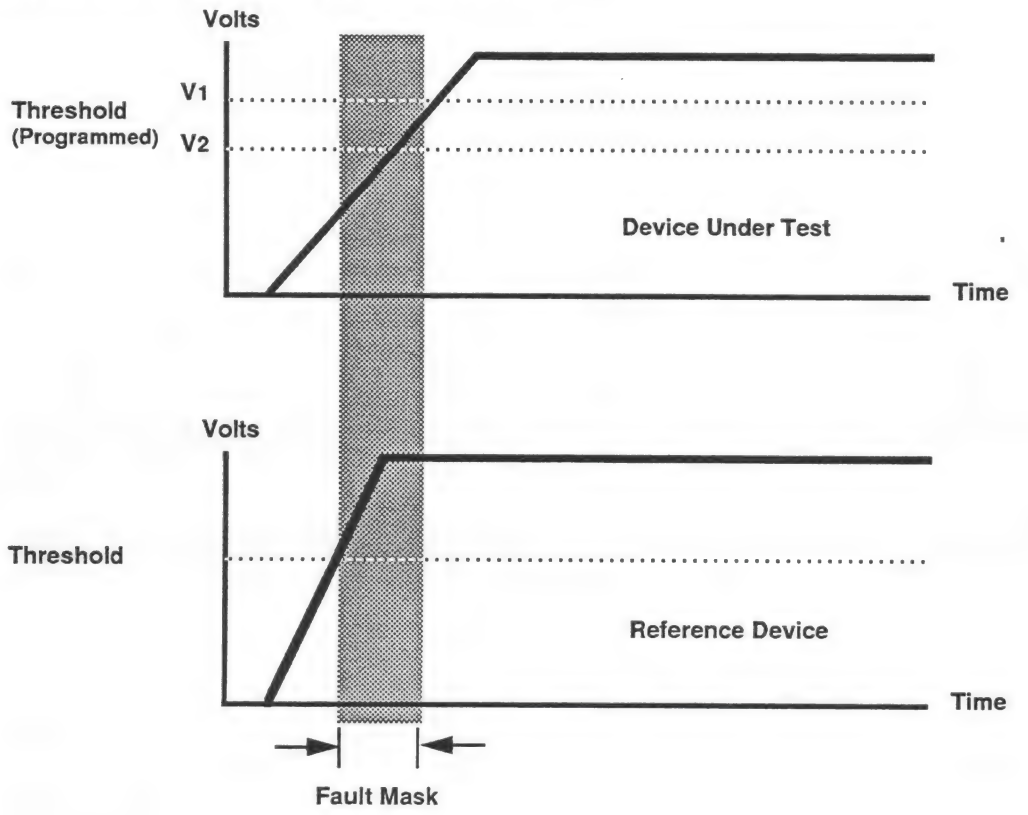



Figure 27

Note also that the Threshold parameter can affect the setting of F_Mask by shifting the apparent edge of the DUT signal. In the diagram, if the Threshold setting were lowered (dotted line V2), it would allow a smaller value of F_Mask to be used. By raising or lowering the Threshold setting, together with changes in the F_Mask, you can select an optimum Performance Envelope (PE) for a DUT. In practice, F_Mask is more often varied to compensate for in-circuit loading, and Threshold is more often left constant.

For typical Sequence development it is found that about 80 percent of the devices on a board pass with no change to the default parameters. For only about 20 percent are changes necessary to account for in-circuit effects such as loading. The rule of thumb is to find the smallest value of F_Mask that will pass consistently, and the value of Threshold that is closest to 1.8 Volts, in order to have the best PE. Once the minimums are established, you may find it necessary to increase F_Mask by one increment to allow for differences between boards. Also, if your F_Mask setting is larger than 70 ns or 80 ns, check to see if changing one of the other parameters (like Gate) will allow you to make F_Mask smaller.

A quick method for determining the PE settings is to use the Learn feature that was added to the 900 operating system beginning with version 6.00. This feature will "automatically" test up to thirty six combinations of F_Mask and Threshold settings.

Remove the fault insertion lead from either pin 10 or pin 14 of U80 (press the red button on the sales demo trainer). If you are presently in a fail screen press [ESC].

Press [F5] (learn) to obtain the following screen.

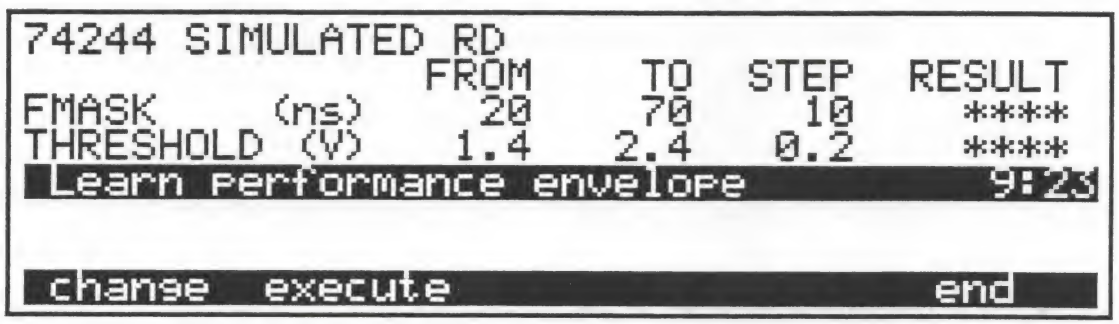



Figure 28

While relying on all other test parameter settings presently in effect, Learn will start with a 1.4 volt Threshold and 20 ns F_Mask and test the DUT repeatedly by increments of these two parameters until it reaches settings of 2.4 volts and 70 ns, as shown above. If these settings are not appropriate, you may select [F1] (change) to alter the default ranges. Once altered to a desirable range, press [ESC] to return to this screen.

Once these settings are acceptable, press either [F2] (execute), or [TEST] to start the Learn.

You should obtain a screen similar to what is shown in figure 29. There may be slight differences in the test results due to performance variations of the unit under test (UUT). On occasion, you may also get a message like "Clip moved during test" as the Learn first starts. This is most often due to a noise spike measured on the Ground pin of the DUT at the low Threshold setting. Simply start the test again.

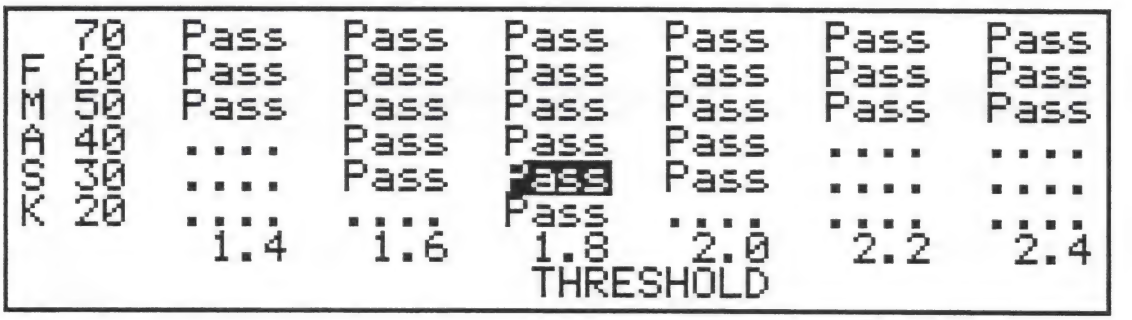



Figure 29

Notice the highlighted Pass result near the center of the screen. This pair of F_Mask and Threshold settings are recommended by the algorithm in the Learn feature as being the best settings found.

Re-attach the fault insertion lead to U80 pin 10 and pin 14 (press fault button F8 on the sales demo trainer).

Once the failure has been re-established, press [ESC] to return to the first Learn screen, and start the test over by pressing either [F2] (execute), or [TEST]. With the failure inserted you will get very few — if any — passes at the default settings.

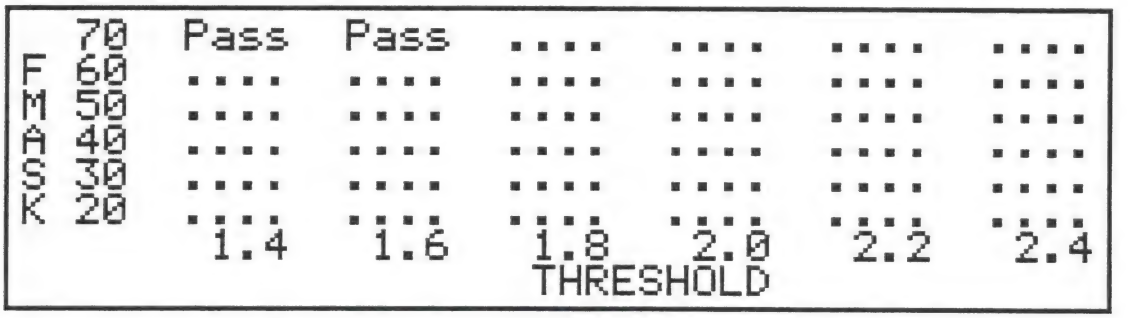



Figure 30

When there are insufficient pass results for the 900 to suggest good settings for F_Mask and Threshold, the 900 Learn algorithm will not highlight a recommended pair of settings. However, in most cases the 900 will make suggestions on how to change parameters so as to obtain better pass results. Press [ESC] once to return the the first Learn

screen, as shown in figure 31.

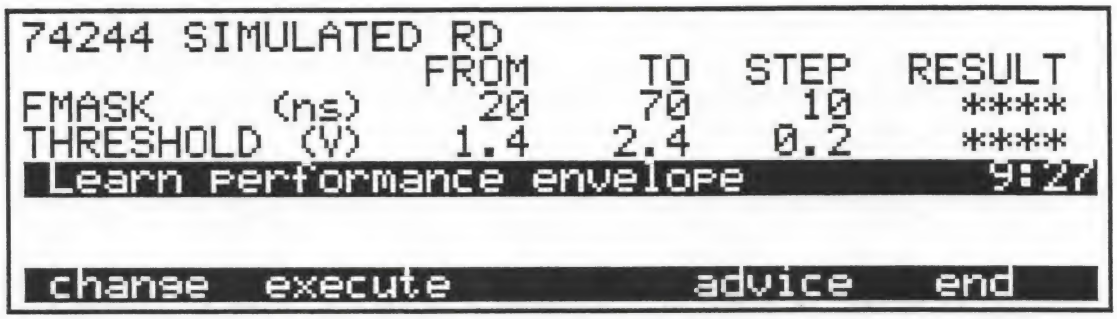



Figure 31

If you examine the function key labels in the above screen, you will discover a selection labeled "advice" that was not previously displayed. This selection is often displayed if the Learn algorithm has insufficient pass results to work with. Press [F4] (advice).


Figure 32

The Learn algorithm was unable to obtain sufficient pass results at the default settings. It is now suggesting that the F_Mask step be increased to 40 ns in order to obtain better pass results for evaluation.

Press [ESC] to leave the advice screen.

Press [F1] (change) to alter the default settings, increasing the FM_step to 40 ns as suggested.

Press [F3] (FM_step). Type in [4], [0], [ENTER]. Then press [ESC].

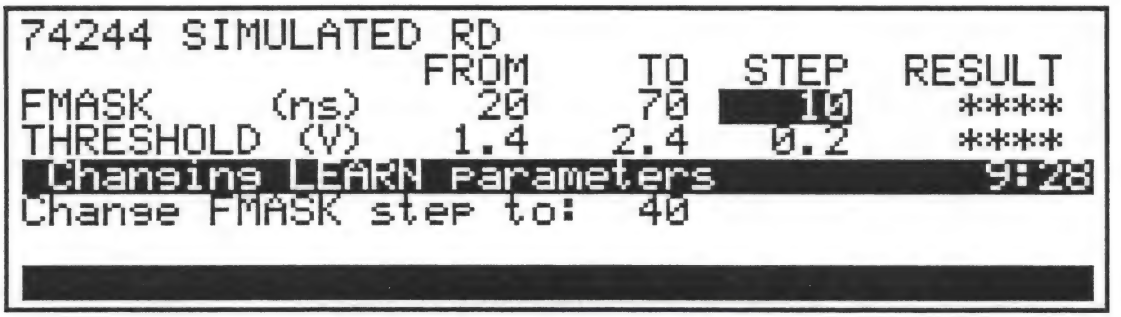



Figure 33

Once again press either F2 (execute), or TEST to start the Learn again. You should obtain quite a few pass results at the new settings.

When Learn has finished testing, and suggested a new pair of parameters, press ESC.

Again you will see that the Learn algorithm has some advice regarding the current parameters. It was able to select an acceptable pair of settings for F_Mask and Threshold, however because of the large FM_step there are probably better settings that could be found. The new advice suggests changing parameters and re-Learning so as to refine the settings to more optimum values. Since we found several pass results at the 70 ns range on the first Learn screen, the quickest way to find better parameters would be to set FM_step back to 10 ns, and set FM_from to 60 ns or 70 ns. Essentially, just move the window of tests up several increments. This change produces the following results.

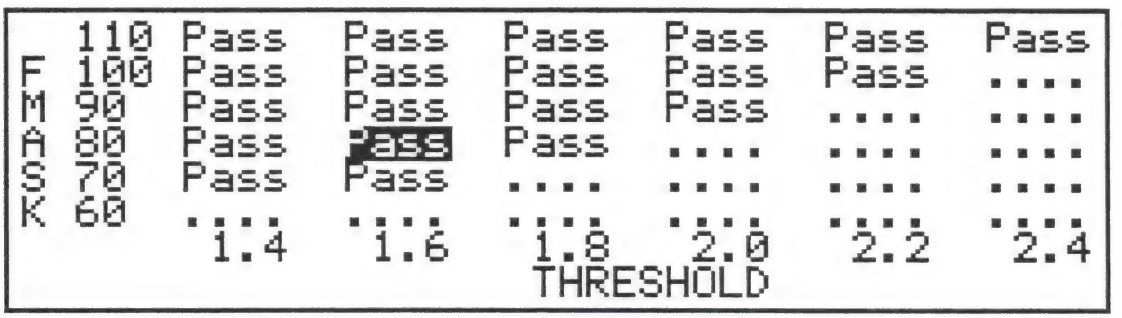



Figure 34

With just a little practice, and by paying attention to the advice screen suggestions, you should be able to establish good settings for the PE quite quickly.

Once test parameters are established during testing of a good board they are stored in a Test Sequence, such as the T900 sequence you are now using. The parameters for each DUT are loaded from storage when the "U" number (or other identifier stencilled onto the UUT) is selected. Selection is done by either typing in the "U" number, or by pressing

the [NEXT] key. If you make a change to a parameter while in run_seq mode, the change is only temporary and does not alter the stored value for that location. For example, after changing F_Mask for U79S, you may restore the original stored value by typing [U], [7], [9], [S], [ENTER] at the 'Ready' prompt. This process of re-loading stored values can also be used to move (or jump), directly to other stored tests in a Sequence (e.g. typing [U], [3], [6], [ENTER] at the 'Ready' prompt would load stored values to allow testing of location U36).

This ability to jump to anywhere in a Sequence by typing in the location name ('U' number) is used by the operator to take a shortcut, and directly call up the test for a device he suspects. The [NEXT] key steps through the Sequence in the order they were programmed.

Starting on a bad board instead of a good board requires much more skill on the part of the operator. It may be that the problem that you are trying to compensate for is the source of the problem on that board. If you are creating a new Test Sequence while working on a bad board, be sure to go back and verify all tests stored once the failure has been located and repaired. Otherwise your confidence in the test procedure will necessarily be lower when working with the next bad board.

Section 3 of this course describes the basic process for creating a Test Sequence.

## 3.2.2 Contention on a Tristate DUT

Press [ESC], [ESC], [NEXT] at this time. The screen on the tester should be:


Figure 35

Move the Test Clip to U64 (use U43 on the sales demo trainer). It is also a 74244, but it exhibits something that is not unusual in some bus driver designs: contention. This occurs when two drivers are momentarily enabled at the same time on a common bus. Logic levels are indeterminate for this period and appear as a fault to the 900. The CPU on the board typically is not accessing the bus during this time, however, and so ignores the apparent fault. The Gate parameter on the 900 must be set to ignore the bus contention also, so it doesn't show a false failure.

Open the TTL Databook to where the description of a 74LS244 is found. Notice from the connection diagram and the function table that pins 1 and 19 are used to turn the outputs of the chip on and off. (Also referred to as Gate enable (turn on), and tristate (turn off).) When pin 1, pin 19, or both are Low, the appropriate output pins are turned on. When one or both are High, the appropriate output pins are allowed to float (tristate), usually to an indeterminate voltage that is recognized as not quite High, and not quite Low. Another booklet, titled Microprocessor Solutions, is included to help in reading and understanding the databook information. The concepts contained in Microprocessor Solutions will also aid a technician in selecting the right parameter(s) on the 900 for a given test.

Press [F1] ( local), [ETC], and [F4] (gate) to show the Gate setting for U64 as follows:

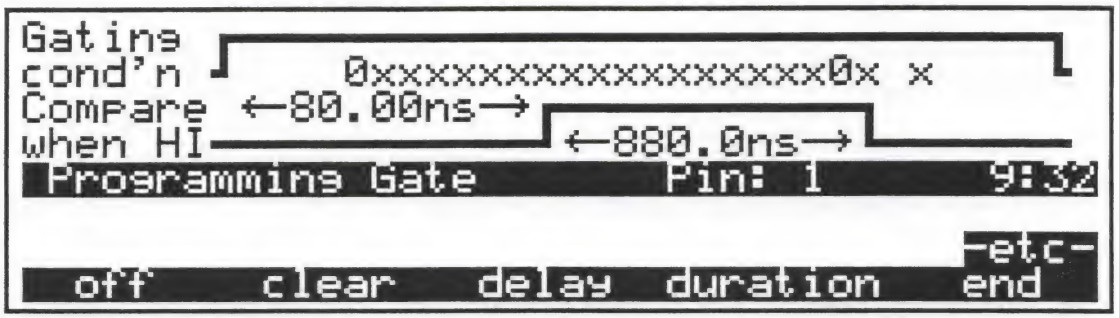



Figure 36

The row of Xs with the flashing cursor represent the pins of the 74244 DUT (from left to right, pins 1 through 20, respectively). There is a space and one more 'x' at the right of the screen. The extra 'x' corresponds to the EXT Patch Lead connection on the Interface Buffer, which may be used at the discretion of the operator. The 0 at pins 1 and 19 mean that this is the logic condition that enables the output of a 74244 - the Gating Condition. Any combination of 0s and 1s entered on the Gate screen must be measured simultaneously on the DUT (must be true), in order for the test to be enabled. Gate may be thought of as "once the test time starts, test only while these conditions are true", and is used for conditions that are required in order for the test to be valid. Most often these signals are repetitive. There is another parameter, Trigger, that is used in a mode that may be thought of as "don't start testing until this is true, and test constantly from then on." Trigger will be discussed later in this text.

Values for the Delay and Duration of testing have been set so that, after the DUT is enabled, the tester waits (delays) for 80 ns before comparing for 880 ns (duration). In this way it avoids the indeterminate signals that contention causes near the leading and trailing edges of the Output Enable signal(s).

In the diagram below note how devices 1 and 3 are enabled briefly at the same time that device 2 is enabled (represented by the shaded areas). Our DUT, U64, is in the situation of device 2 of this example. Since the CPU is not using the bus during these brief moments of contention, there is no noticeable effect of the contention during normal operation. As boards with this type of design age, the periods of contention tend to increase because of minor damage to the bus driver chips. In most cases the contention must become quite significant before there is a failure of the board.

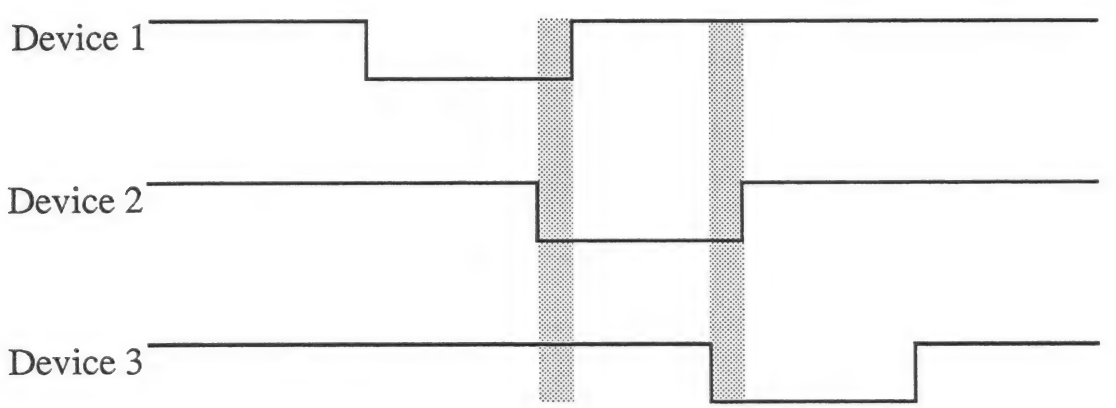



Figure 37

For the current test on U64, test values of delay and duration have been set that limit testing to a portion of the time that the device is enabled. An alternative method for Gating is to connect the EXT Patch Lead to a signal elsewhere on the board. The EXT lead must be connected to a signal that defines a "valid" time window during the time that this device is enabled. In effect, the EXT signal will then be used to further limit testing instead of using the delay and duration parameters. Unfortunately, use of the EXT lead for this purpose requires greater knowledge of the circuit. Below is a diagram that shows how use of another signal on the board can be used to help Gate a test.

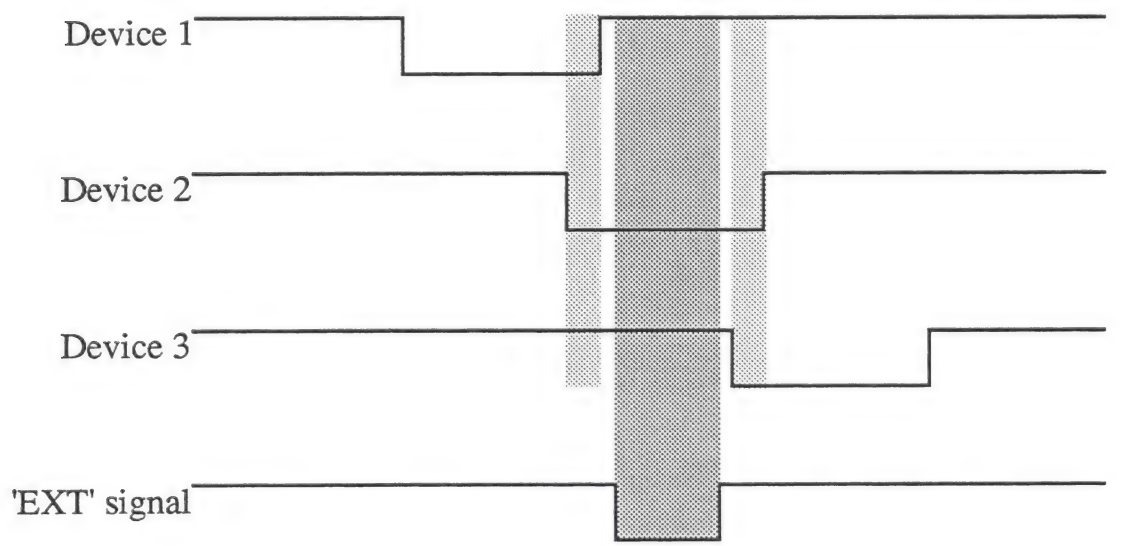



Figure 38

Normally there is one, or sometimes two signals on any given board that will define this

"valid" time window. Common signals to look for are Address Latch Enable (ALE), Data Latch Enable (DLE), Read, Write and some type of phase clock. Care must be taken when using Read and Write, as this tests a device in only one "direction." After finding a candidate for an EXTernal Gate signal, it is a good practice to induce a failure (such as a capacitive delay) on the outputs of the device to verify that the selected signal is the right one.

Press [F1] (off), and [F5] (end) to disable the Gate setting.

Press [TEST] and observe the FAIL DUT result.

You may re-enable the Gate setting to obtain a PASS. Press [ESC] to leave the Fail screen, [F4] (gate) to enter the Gate setting mode and [F1] (on), [F5] (end) to re-enable the previous setting.

Pressing [TEST] should now result in PASS.

At any time during the operation of the 900 that a selection of [F5] (end) is displayed, you must select 'end' after making desired changes in order to keep those changes. Pressing [ESC] without pressing [F5] (end) will discard the changes made. It is good practice, unless there is some reason not to, to use Gate on the enable pin(s) of any device that is capable of tristate conditions — even if the enable pins are tied to Vcc or GND. In the event that the device is never selected, the 900 will then announce that comparison never took place. Advice on how to set the Gate is found in the 900 Operator Manual, Appendix I under Bus Device Applications.

# 3.3 Testing Synchronous Devices

*This subsection covers the testing of synchronous devices, those ICs that have clocked inputs. The 900 employs techniques to put such RD devices as counters and latches into the same state or phase as the DUT before they are compared. An example of a standard device is shown as well as a custom PAL device. The most common parameter change to handle timing race difficulties on synchronous devices is illustrated.*

Synchronous devices have outputs that depend not only on immediate input signals, but also on previous input states that were clocked in. The success of Dynamic Reference Comparison rests on the tester knowing the internal state of the DUT, so that the RD can be matched to it before comparison. For devices such as flip flops and counters, this means monitoring the output and clock pins. For devices such as shift registers with hidden states, this means monitoring the inputs while those states are being clocked in. The information on how to synchronize a specific RD and DUT is part of the library information for that device type and is done automatically for the user. If you create a custom library for a synchronous device, you will need to specify how to synchronize it in your library entry.

Press (NEXT) from the U64 screen to proceed to the next test. The screen of the tester should appear as follows:


Figure 39

Clip over U4 (use U27 on the sales demo trainer). Do not worry that the 24 pin Test Clip contacts pins on another device since the tester ignores the extra pins, provided pin 1 is in the right place. Press (TEST) and observe the status line during test. At the start of test it indicates that the tester is synchronizing the DUT and RD for a period of time before comparison testing begins.

After the PASS result press (F1) (local) to see the parameter settings.


Figure 40

Notice that STIME (Sync Time) is set to 3000 milliseconds. This means that the tester will try and match the RD and DUT for ***up to*** 3 seconds before timing out. Normally, synchronizing takes much less than that, depending on the activity on the board. If synchronization is accomplished in less than the maximum time allowed, any remaining time is truncated and comparison starts immediately.

## 3.3.1 Timing Race on Synchronous Devices

*Occasionally, the circuit around a synchronous device like a flip-flop provides input data transitions that are very close to the edge of the clock signal. Recall from the diagram of the Performance Envelope that changing the Threshold setting can shift the signal edges. It is therefore possible to shift the edge of the input data to one side or another of a clock edge. In this way a 7474 RD could clock in a 1 or 0 depending on the Threshold setting. The Threshold should be chosen so that comparison passes on a good board.*

Change the Threshold setting for U4 to 1.4 volts, press [F3] (thrsld), [1], [.>], [4], [ENTER]. Test and observe the result. You should see pins 8 and 9 failing.


Figure 41

Open the TTL Databook to where the description of a 74LS74 is found. Notice from the connection diagram that both the Q and complement Q outputs are failing. This is characteristic of a race problem where RD and DUT are out of phase. Another clue is that no small change of F_Mask will cause a PASS result, as would be the case for simple in-circuit loading. For example, you can increase F_Mask to 100 ns and there will still be a failure. The correct adjustment is to increase Threshold to 2.1 volts to shift the signal edges and permit a PASS result with a small F_Mask value.

To verify this adjustment, press [ESC] twice to leave the fail screen and return to the manual menu, where learn is available.

Press [F5] (learn), and either [F2] (execute), or [TEST] to start the Learn. A suggested setting will be around 2.2 volts and 40 ns.

To refine the adjustment, change the TH_step to 0.1, and the TH_from to 1.8 volts. Re-learn with the altered range. Your results should indicate a suggested setting of about 2.1 volts and 40 ns. When you leave the Learn screen, be sure to select [F5] (end) to store the new settings.

## 3.3.2 Testing a Synchronous PAL Device

*Programmable Array Logic devices (such as 22V10), have a standard set of logic blocks that are programmed by the designer to implement a custom function. These devices may be tested by the 900 without knowing their function, as long as a good device is available for use as an RD. The letters PAL are required as part of the device description (PAL22V10) because that is the naming convention used in the 900 Library. Appendix IV of the Operator Manual lists all of the devices available in the current Library, and the name they are known by.*

Press [NEXT] to bring up the next test and [F1] (local) to display its test parameters. Insert the DEMO3 PAL RD into the ZIF socket and clip DEMO3, which is found on the UUT daughter board that is plugged into U1 (the math co-processor socket). (If you are using the sales demo trainer, DEMO3 is found on the fault insertion board.)


Figure 42

Press [TEST] several times and observe the pattern of failing pins. They should display a different failure pattern every time. This is typical of a synchronization problem. Had this been a Performance Envelope (PE) problem, the failure would have remained constant. This PAL is configured to be a free-running counter that has no reset, clear or preset pin. This situation is difficult to test by any technique since the device cannot be initialized. The test parameters were not completed in the Sequence, and it has been left for you to enable Sync Time with a large enough value to produce a PASS result. Press [ESC] to leave from the FAIL screen. Then press [ETC], [F2] (s_time) and type in the value 5000. Test again and observe the Status Line for an indication that DUT and RD are first synchronized before being compared.

As noted earlier, if all of the value for STIME is not required any remaining time will be disregarded once synchronization has been achieved. The direct consequence of this is that, unlike the parameter FMASK, STIME can — and probably should — be set longer than necessary. In order to comparison test the DUT, it must first be synchronized to the RD. If insufficient time for synchronization is allowed in a test sequence, the technician will probably spend considerable effort discovering that fact. The technician may even

be led to replace good chips because of a synchronization failure, when in fact the only problem was that more time was required for synchronization.

Try setting STIME to 9990 to verify that "extra" time is not used. If it was, then synchronization would take almost 10 seconds.

## 3.4 Testing Programmable Devices

*This subsection shows the testing principles for programmable devices. These devices have many hidden states and may have indeterminate outputs until initialized by certain signal activity. The use of the Trigger parameter to initialize a 8259 Interrupt Controller will be examined as well as the use of the Shadow parameter to ensure initialization of a RAM device.*

### 3.4.1 Triggering on DUT Initialization

Press (NEXT) from the DEMO3 Sequence screen to continue to the next test.

The following screen should appear on the tester (if you are using the S900 test sequence with the sales demo trainer, the message about JP10 will not be present):

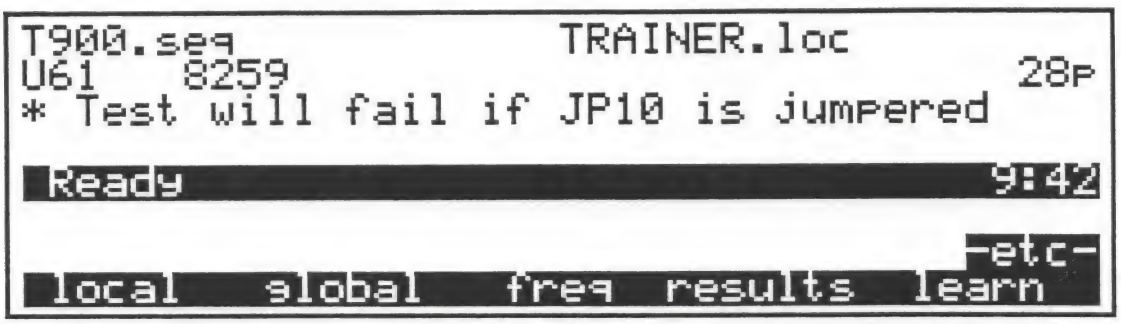



Figure 43

Place the 8259 Reference Device in the ZIF socket and insert the 28 pin Test Clip in the Interface Buffer.

Clip over U61 (on the sales demo clip over U62). On the self-paced trainer remove the jumper shorting plug from the connector block labeled JP10 before testing this device. The test parameters are optimum for testing the 8259 in the lower speed configuration that this change enables. The sales demo trainer requires no adjustment.

Press (TEST) to obtain a PASS test result.

Move the jumper shorting plug from JP10 to JP8 (where the RST and GND Patch Leads are connected). This grounds the board reset line, disabling the CPU. (If you are using a sales demo trainer, press Fault Switch 2). If this fault is properly inserted, the LEDs on the UUT will stop counting. Press (TEST) to start the test, and observe "Waiting for Trigger" on the Status line. The 900 will continue to wait for the required trigger forever, unless interrupted.

Press [TEST] again to stop the test.

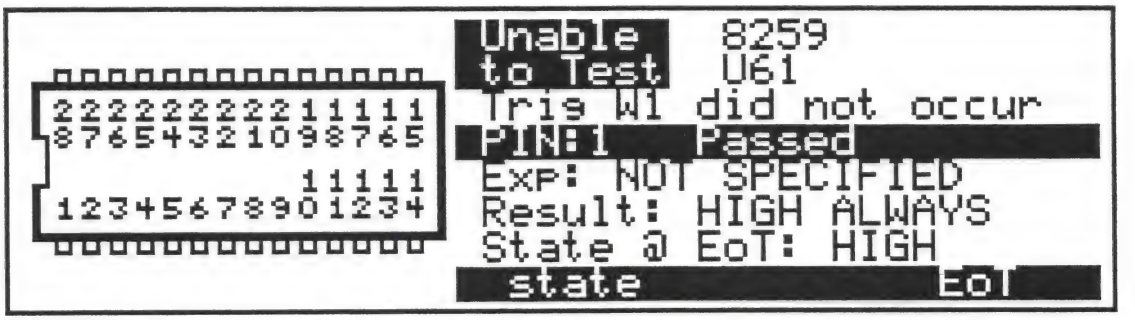



Figure 44

The test result tells us that comparison testing was not done (Unable to Test), because Trigger word 1 (Trig W1) was not received by the DUT. This indicates that the user should backtrace to a device feeding U61 to find the problem.

Press [ESC], [F1] (local), [ETC], and [F3] (trigger) to display the setting for Word1 and Word2.

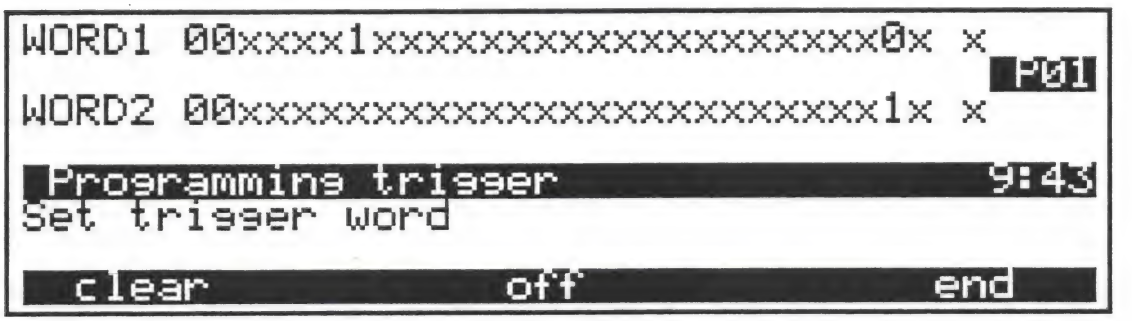



Figure 45

This screen is similar to the Gate screen, except there are two "words". The pattern of 0s and 1s shown for word 1 must all be measured simultaneously on the DUT before that condition is satisfied. After word 1 is satisfied, the 900 begins waiting for the conditions specified in word 2 to be satisfied. Both words must be satisfied, in order, before testing is allowed to start. Any pin that is specified as an 'x' is a "don't care," and will be treated as if the condition on that pin was satisfied. After both words are satisfied, and unlike the Gate parameter, testing will take place continuously until either a fault is detected, or the test time expires. Trigger and Gate use the same register in the 900 and are thus mutually exclusive. They may not both be used on a single test.

For this test, certain pins states are set to 1 or 0 according to the data book definition of the command words for this device. The 8259 outputs are indeterminate until the

processor writes command words to its control registers to define its operating modes. The Trigger is set to a "write" taking place at the address of these command words, and comparison of RD and DUT will not start until they have appeared. The exact control words for this board are not known. The Databook for the 8259 indicates that the addressing of the control registers is unique, and could be used as the Trigger without actually knowing the data that was written into them.

The following information from the databook was used to develop the Trigger words for this test:

Chip Select (pin 1) – A Low on this input enables the 8259. No reading or writing of the chip will occur unless the device is selected.

Write (pin 2) – A Low on this input enables the CPU to write control words to the 8259.

$A_0$ (pin 27) – This input signal is used in conjunction with Write and Read signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

General – Before normal operation can begin, the 8259 must be brought to a starting point by a sequence of 2 to 4 bytes timed by Write pulses. Whenever a command is issued with $A_0$ = Low and D4 (pin 7) = High, this interpreted as Initialization Command Word 1.

Remove the fault from the UUT by moving the jumper shorting plug back from JP8 to JP10 (or press the red button on the fault insertion board if you are using the sales demo trainer).

## 3.4.2 RAM Shadow ensures Initialization

Two RAM devices were provided with this course. Place the smaller device, the 16 pin 41256 RAM chip, in the socket (it may have slightly different numbers on it, such as 4256, or 51256).

Press (ESC), and (NEXT) to bring up the next test.

The Shadow parameter is enabled from the RD menu level, and records all the addresses written to the RAM during a test. This does not mean that the data written to those address are recorded, only the fact that specific addresses were observed to be written to. Only those addresses that are first written are permitted to be compared when they are later read or written again. This avoids "false failure" test results from board activity performing a read-before-writing (under program control, or induced by the board fault). Remember that both the RD and the DUT must be initialized to the same values before a valid comparison can take place.

Insert the 24 pin Test Clip and clip over U70 (recall that a test clip that is larger than the device being tested may be used as long as pin 1 of the clip lines up with pin 1 of the device, and all pins of the device are firmly clipped). (On the sales demo trainer, clip over U90.) Press (TEST) and observe a test done in four passes, pages 0,1,2, and 3. The high speed Shadow RAM is 64 Kbyte in size and, therefore, the 900 must test the 256 Kbyte DUT in four passes.

After obtaining a PASS test result, notice the message just below the Status line that reads "Addresses written: 262138." (Your results may vary slightly.)

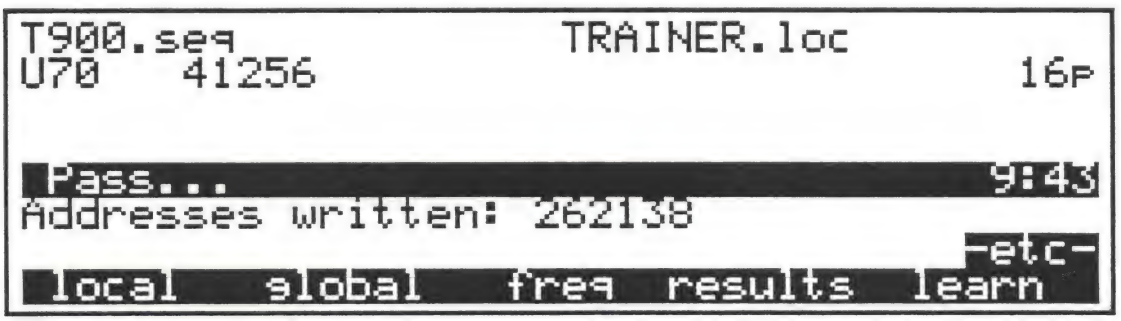



Figure 46

When Shadow is used the total number of different addresses written during the preceding test will be displayed. The indication of the number of address locations written tells us how complete the RAM test was. In this case, most cells in the 41256 RAM have been tested (256 x 1024 = 262144). Had the stimulus been slightly more thorough, the whole device could have been tested.

Remove the RST lead temporarily from the UUT and re-execute the test. Observe again the number of address locations written. (Your results may vary.)

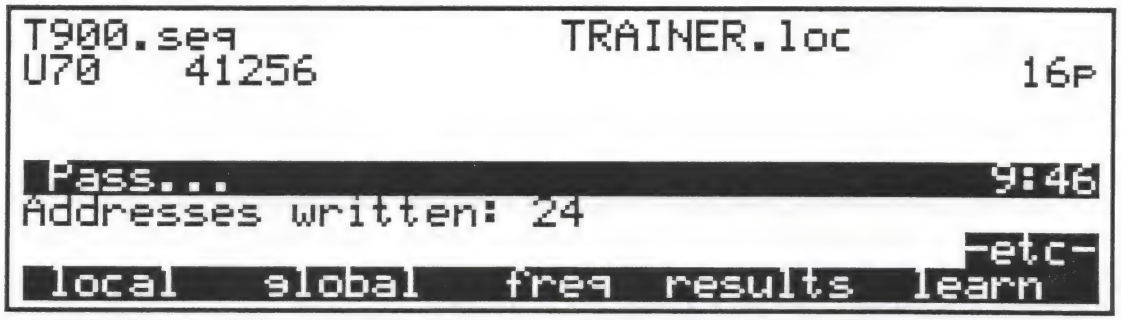



Figure 47

Re-attach the RST lead before proceeding.

When the test was executed without the RST lead, the on-board self test was not initiated on the UUT. The 24 locations written to were probably used by the BIOS routine on the UUT for temporary register or stack storage. Because of the low number of addresses written to, this RAM was essentially untested by the test done without the RST signal. The stimulus activity is very important in ensuring a good quality of test. For RAM, this often means using Reset, or looping through a full RAM diagnostic.

If a RAM device is not included in the 900 Library with a RAM Shadow, then testing it will require more information from the 900 operator. In such situations use of the Trigger is appropriate. As with the Shadow, it is important to test only those locations in the RAM that have been initialized. Testing locations that are not initialized will result in false failures because the data stored in that cell of the DUT has only a 50% chance of being identical to the data stored in that cell of the RD.

Most RAM diagnostic programs will either test RAM starting at the lowest address and going through each cell until the highest address has been tested, or the reverse. On occasion, for speed in booting up a board, the programmer will only spot check to ensure that there is RAM installed beyond specific logical boundaries. If spot checking is done, testing may prove to be impossible without a RAM Shadow. In the first instance testing may be accomplished by setting a Trigger to watch for completion of the first pass through RAM. This is done by setting all address pins to either 1 or 0 (try both ways), while the select and output enable lines are True.

Press F1 (local), ETC, F3 (trigger) to see the screen shown in figure 48.

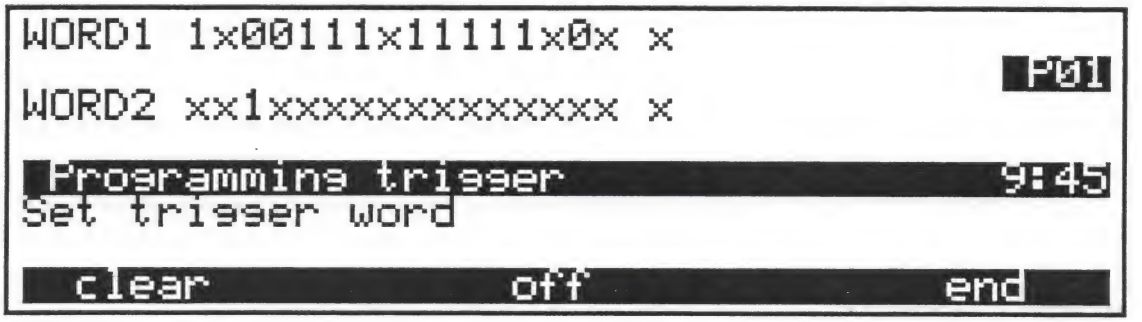



Figure 48

This Trigger is loaded, but has been disabled since a RAM Shadow was available. For Word1 all of the address pins have been assigned a value of 1, to trigger on a write to the highest address of this device. The enable pins (pin 4 and 15) have been set to 0, or True, while pin 3 (Write) is True. On Word2 the only thing we are looking for is to see that the Write operation was completed at the address above. Note that no values are assigned for the data pins (2 and 14) because we do not know what data may be written, nor is it important. The only thing that is important is that both the DUT and the RD receive the same data.

If this Trigger were used for testing instead of the Shadow, there are three possible results. First, the RAM could pass comparison. Second, the RAM could fail comparison. If this happened, the device is probably bad. Third, the Trigger could fail to occur. If this were the result, then there is a failure in the board closer to the microprocessor, or to the edge card connection on non-microprocessor boards. What ever the failure is, it is preventing the Trigger condition from reaching the RAM.

# 4 Secondary Conditions Testing

*This subsection provides examples of the measurement capabilities of the 900 and their use in providing secondary test results. They may be used to help interpret the primary DRC result or they may be used on their own where DRC testing is not possible. The types of conditions that may be verified include checks that a pin is High, Low, Active, has a specific Frequency and that it attained a specified voltage level. In addition, the Trigger, used previously to ensure initialization, may be used to detect logic events on all pins of a device.*

Press (ESC) to leave the Trigger screen for U70. Press (NEXT) to load the test for U40.

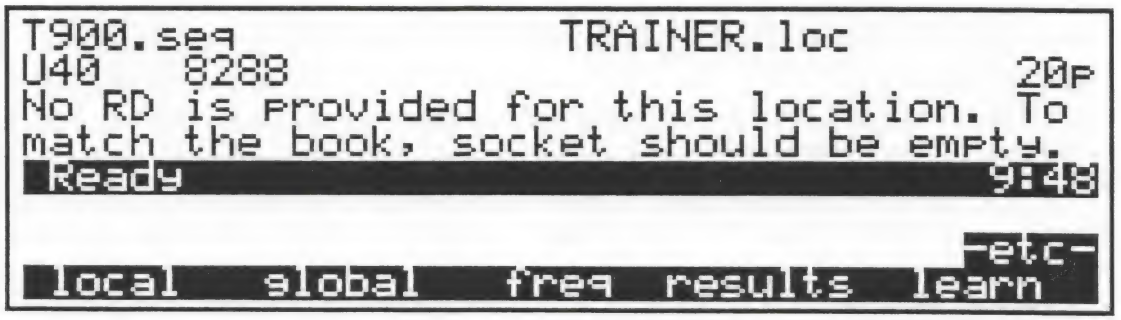



Figure 49

Note that the socket should be empty and no device is simulated. Condition testing does not use RD comparison, although it may be done simultaneously with a comparison test.

Insert the 28 pin test clip, clip over U40 (use U2 on the sales demo trainer), and press (TEST). The test should pass.

Now remove the jumper shorting plug temporarily from the connector block labeled JP10 (or press the fault insertion button labeled F1 if you are using the sales demo trainer), and re-execute the test. This fault changes the board clock speed by changing a control signal on the 8284 clock generator. On the self-paced trainer the speed decreases, on the sales demo trainer the speed increases.

Press (TEST).


Figure 50

Note that the result is FAIL *Conditions* (versus FAIL *DUT* for comparison test). The actual frequency on pin 2 was different from the expected frequency programmed into the Sequence. This would tell the user to backtrace to the oscillator circuit to find the source of the problem. Refer to the 900 Operator Manual Section 3.3.4 for information on how to set expected pin conditions through the pin_def parameter.

**Summary**

In most situations Conditions tests are placed on the inputs to a DUT, since the outputs are compared to within the limits of the Performance Envelope. The failure of an input condition test implies that the DUT has not received the expected inputs; this should direct the operator back to an earlier part of the circuit to locate the problem. Thus, only if a DUT comparison failure is recorded should the operator be led to believe that the current DUT is the source of the failure.

# 5 Manual Frequency Measurement

In figure 50 the input pin 2 conditions test failed. The test that had been programmed for that pin was to measure 10 MHz, with a 1% tolerance. You may make a manual measurement of frequency at any time.

Press [ESC] if you are still viewing the fail screen.

While in the Sequence screen of U40, press [F3] (freq) and specify the pins to be viewed: [1], [F1] (thru), [8], [ENTER].

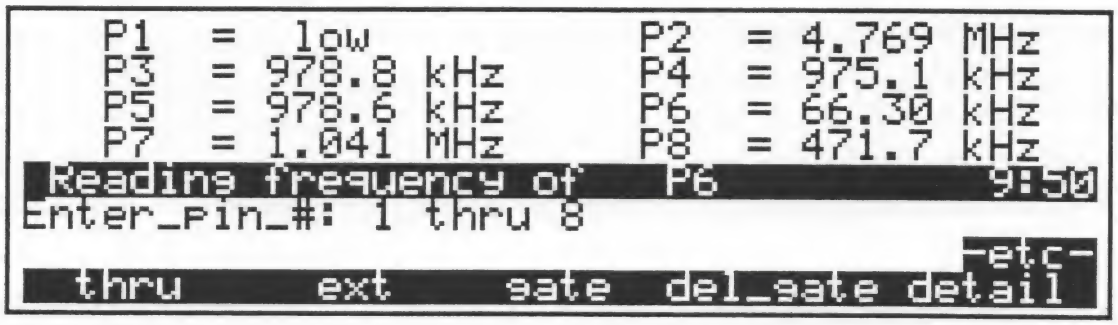



Figure 51

While this measurement test is running, restore the jumper shorting plug to JP10, (clear fault F1 from sales demo trainer by pressing the red button). Note the change in frequency measured on pin 2.

You can view timing information on the signals by pressing [F5] (detail), [ENTER]. Note that "/detailed" was added to the current command, then you re-executed the command.

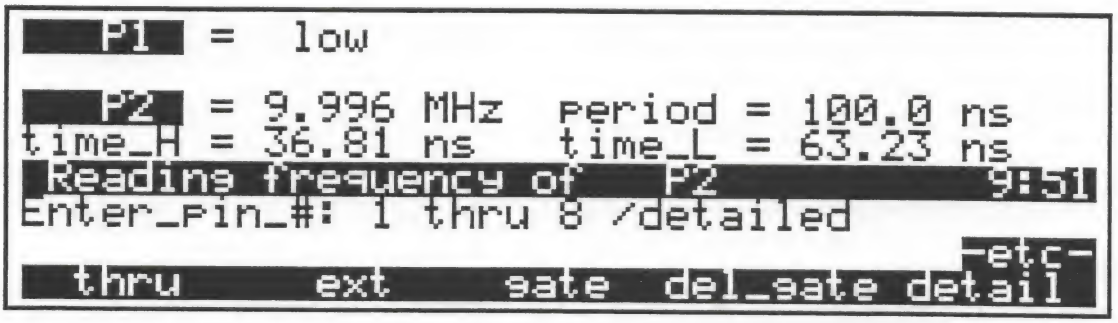



Figure 52

The up/down arrows scroll through pin selections. Shift/up or shift/down lets you scroll four lines (one screen) at a time. Any series or combination(s) of pins may be measured by entering the desired pin number(s), ensuring that there is a space between each to separate them.

# 6 Testing Devices larger than 28 Pins

Press [ESC] to leave the Frequency Mode.

Press [NEXT], insert the 28 pin Test Clip in the Interface Buffer and clip over the lower half of the 8088 CPU chip. Pin 14 of the clip should register with pin 20 of the chip.

Press [TEST] to execute a conditions test on 28 pins of the 8088 CPU.

Try removing the JP10 jumper shorting plug to cause a conditions test failure for wrong frequency (press Fault Switch 1 on the sales demo trainer).

Try moving the JP10 jumper shorting plug to JP8, (press Fault Switch 2 on the sales demo trainer) to observe the missing activity that occurs when reset is held.

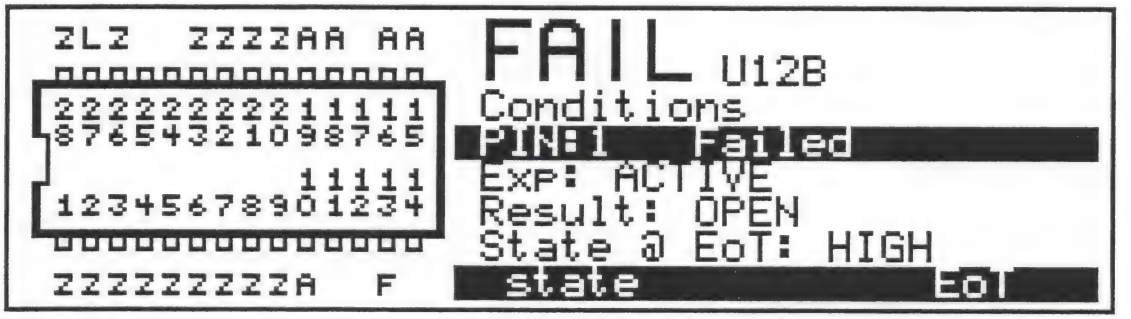



Figure 53

The data and address lines were set to "must be Active," a status line to "must be Low", and the clock pin to an expected frequency. Since a comparison test is not conducted, care should be taken to set conditions for critical input *and* output pins. For this type of test, the size parameter is set to 28, RD Test disabled and Clip Check disabled. The "Z" character indicates floating pins, and is described fully under Float Check in Section 4.

Restore the jumper shorting plug to JP10, or press the red button on the sales demo trainer.

# 7 Device Categorization

*In order to properly select and apply 900 test parameters, it is necessary to understand how devices are categorized. Failure to correctly categorize a device will cause improper test parameter adjustment, possible invalidation of test results, and increased test development time.*

**Device Categories**

For the purpose of comparison testing, devices are classified into three types:

**Combinatorial**
Devices whose outputs reflect – immediately – the conditions on the input pins. They have no internal memory, but may have tristate output pins (e.g. NAND gate, Bus Driver).

**Synchronous**
Devices with internal memory whose state cannot be observed or inferred from an output pin. They always have a clock input line (e.g. up/down counter, Flip Flop)

**Programmable**
Devices that require data to be written into them before outputs are valid (e.g. Interrupt Controller, RAM). In general, these devices have internal hidden memory states.

Try and put the following devices into their categories:

74280, Odd/Even Parity Generator
2764, EPROM
74161, 4 Bit Binary Counter
7491, 8 Bit Shift Register

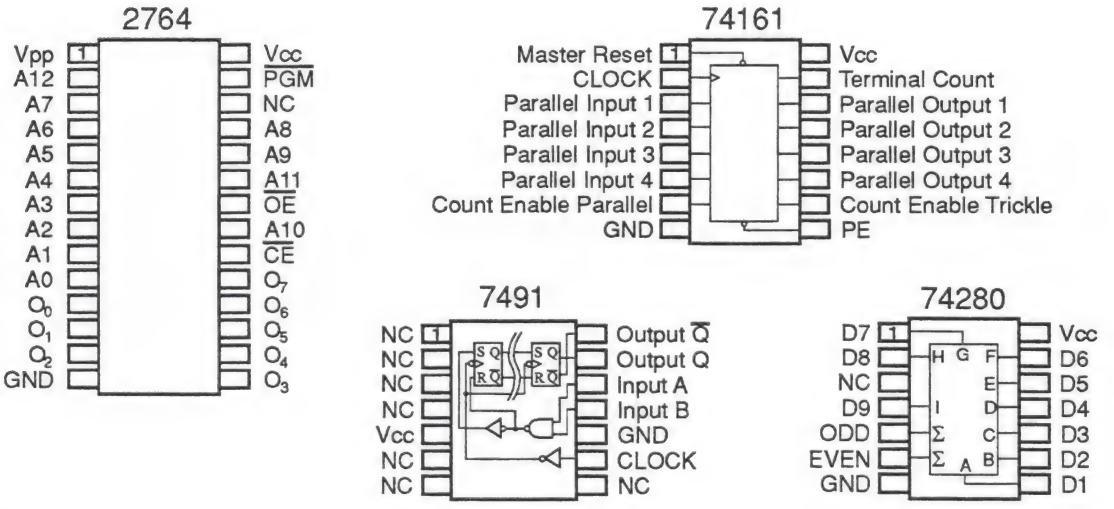



Figure 54

**Answers:**

74280 is a Combinatorial device. Many complicated devices and PALs fall into this category and are simple to test.

2764 is tested as a Combinatorial device because, once it is programmed, the address inputs always produce the same immediate data outputs.

74161 is a Synchronous device because it has a clock input and no hidden states.

7491 can be tested as a Programmable device since 7 of the 8 internal Flip Flops have hidden states. Large FIFO memories have this shift register construction and are considered Programmable. The 7491, since it is a short register, can also be tested as a Synchronous device by monitoring the clock input (pin 9) for 7 pulses on the DUT (see Section 5 on Library synchronization commands). The tester monitors the A,B data inputs during the clock pulses and thus infers the internal states of the Flip Flops.

# 8 Test Parameters

A number of test parameters have been changed in the exercises so far. They may be put in three groups:

Parameters for defining a device.
Parameters to initialize RD and DUT to the same state.
Parameters of the Performance Envelope.

For parameters associated with each of these three groups there will be different error messages generated by the 900 in the event a problem was detected. The logical grouping of test parameters shown below will help to reduce test development time. The proper use of these test parameters is explained in Section 4 of this manual, and also in the 900 Operator Manual.

**Parameters For Defining a Device**

| | |
|---|---|
| IC Name | Example: 7400. |
| Size | Number of pins. |
| RD_Drv | Reference Device ability to drive 1 LS load. |
| RD_Sim | Simulation of Reference Device. |

**Parameters For Initializing RD and DUT**

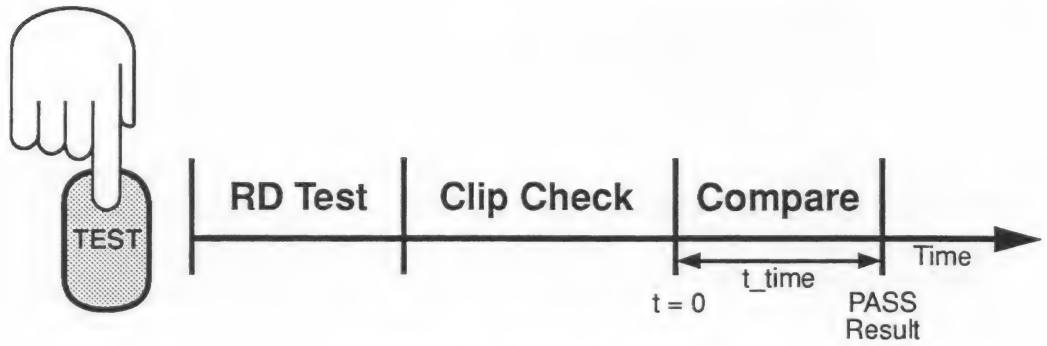
| | |
|---|---|
| Reset | Pulse issued on the RST patch lead to reset a board. |
| S_Time | Sync Time synchronizes RD and DUT devices. All synchronous and some programmable devices use this. |
| Trigger | Starts comparison after a user-defined state appears on the DUT. |
| Shadow | Inhibits comparison at RAM addresses that have not been previously written. |

**Parameters of the Performance Envelope**

| | |
|---|---|
| T_Time | Test Time defines the duration of comparison. |
| F_Mask | Fault Mask defines how close to compare RD and DUT |
| Thrsld | Threshold defines logic 1 level. |
| Pin_Def | Pin Definition permits specified DUT pins to be ignored, or is used to define secondary test conditions (such as required **Hi**, **Low**, **Active**, etc). |
| Gate | Gate enables and disables comparison from a user-defined "data valid" condition on the DUT pins and EXT patch lead. |

# 9 Test Cycles

A diagram is shown below of what happens after you clip onto a DUT and press TEST. It is known as a test cycle diagram.




**Basic Test Cycle**

Figure 55

Notice that RD Test and Clip Check are performed first. This always occurs (unless rd_test or clip_chk are off) so we will omit showing it in further test cycle diagrams. The Time-to-Fault value in the test result is measured from the start of comparison (t=0).

**Reset Pulse**

The reset pulse may be selected to initiate the stimulus for the test (as you have been doing for the tests in this course). The RST Patch Lead is in a tri-state condition until a reset pulse is required. The RST signal is driven to the non-reset level for 10 ms, to the required reset level for the duration specified, back to the non-reset level for 10 ms, and then returned to a tristate condition.

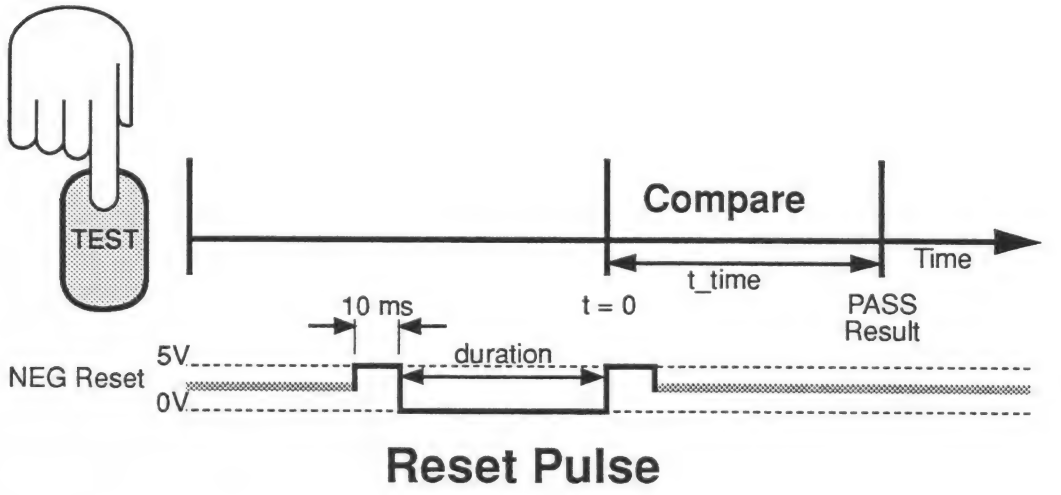



Figure 56

**Reset Offset**

The Reset pulse has a definable duration (100 ms by default) and a polarity which can be positive or negative. The pulse may also be shifted relative to the start of comparison by assigning a value to the Offset parameter found on the reset menu. Shown in the first part of the diagram (figure 57 (a)) is a negative offset (e.g. -30 ms). This time margin after Reset, during which comparison is inhibited, is used to wait for certain programmable devices to be initialized by onboard activity.

A positive offset is shown in the second part of the diagram (figure 57 (b)). It is used only for devices that must be compared during the reset pulse itself (e.g. the board's reset circuit).

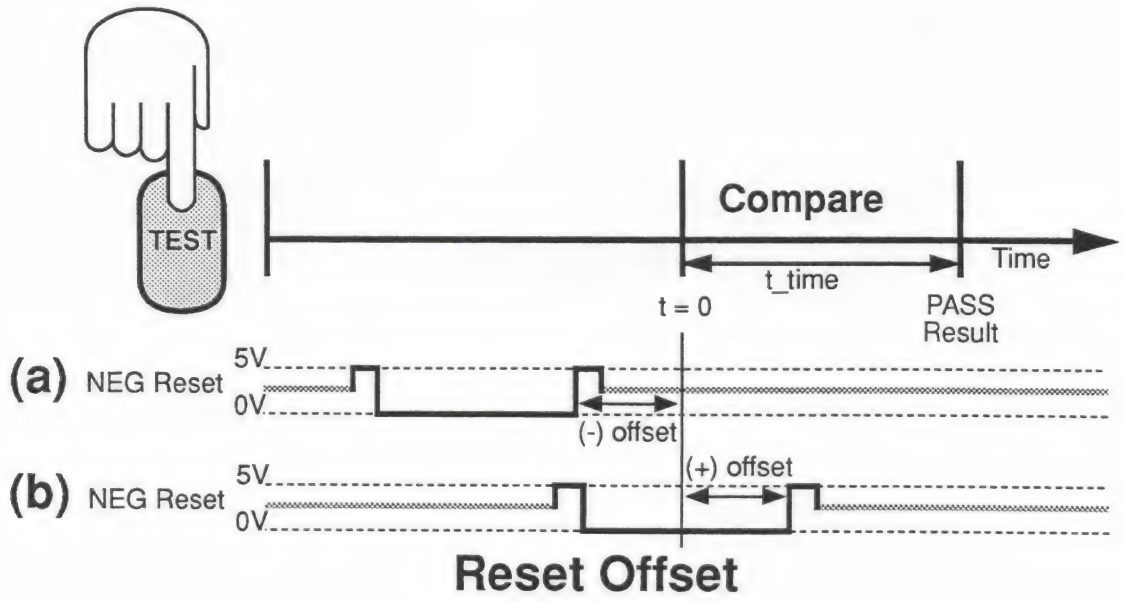



Figure 57

**Trigger Parameter**

Comparison may also be offset for initialization purposes using the Trigger parameter.

Trigger effectively offsets comparison until two specified logic state events appear on the DUT pins or the EXT patch lead.

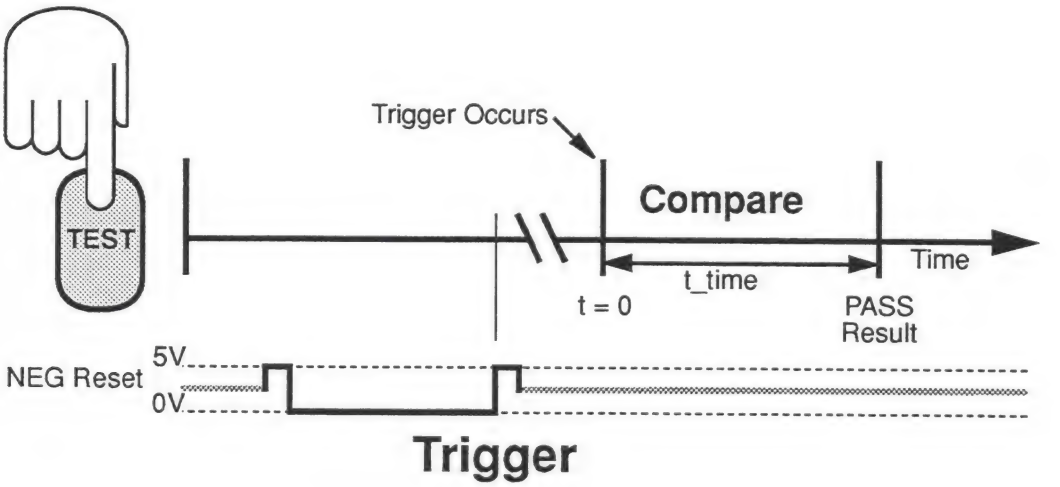



Figure 58

**Synchronization Time**

When the S_Time parameter is enabled, multiple resets are issued while library-resident synchronizing techniques are employed. S_Time is an interval that lasts only long enough for the DUT and RD to be put into the same state. Two types of technique are employed during S_Time:

Method 1
For an active DUT, signal activity is checked for a condition that would guarantee that the DUT and RD are synchronized (e.g. pulse on a Clear pin).

Method 2
For an inactive DUT, the RD is separately stimulated through all its states until its output pins match the DUT.

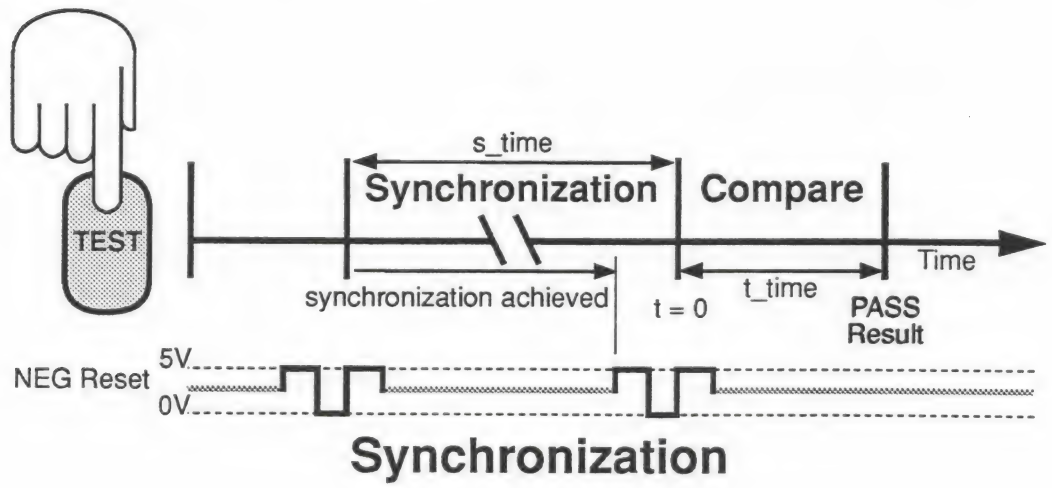



Figure 59

**Gate**

During the comparison interval (T_Time) for all the test cycles, the Gate parameter can selectively enable or disable comparison based on a specified state of the DUT pins and the EXT patch lead. This can be useful to define a window of valid activity on some bus devices. (See Section 2, part 3.2.2, Contention on a Tristate DUT.)

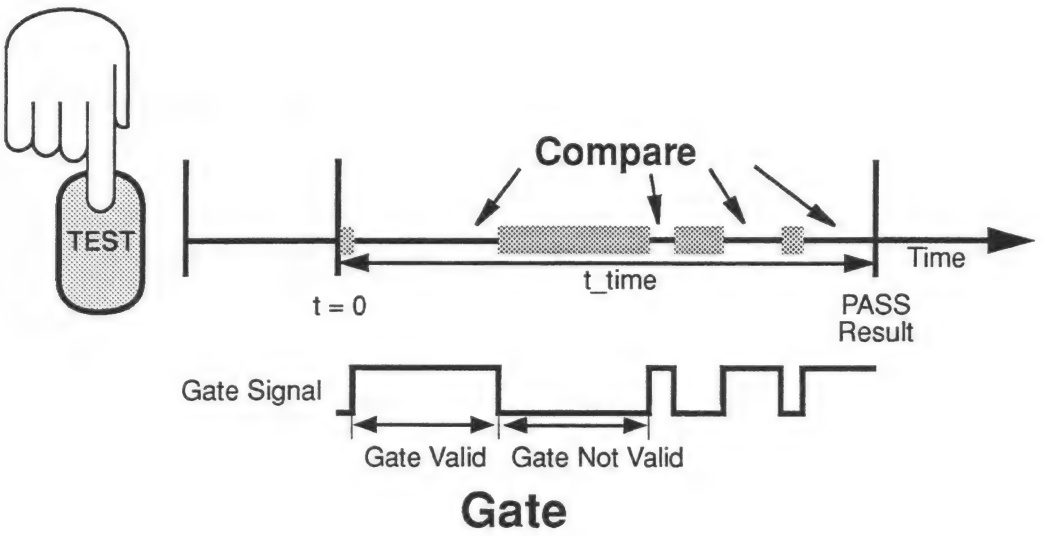



Figure 60

**Default Test Cycles**

Recall that devices fall into three general categories:

Combinatorial - outputs are a function of its immediate inputs
Synchronous - clocked ICs without unknown states
Programmable - ICs with unknown internal states

When a device is selected by generic number, the resident library information sets up the appropriate test cycle. Variations in test cycle from the library default settings are usually only necessary for some programmable devices because of their special application in a circuit. Library definitions for new devices may be added by the user as will be shown in Section 5 of this course.

As an exercise, match the test cycles (A,B,C) with the type of device below:

Synchronous _____
Programmable _____
Combinatorial _____

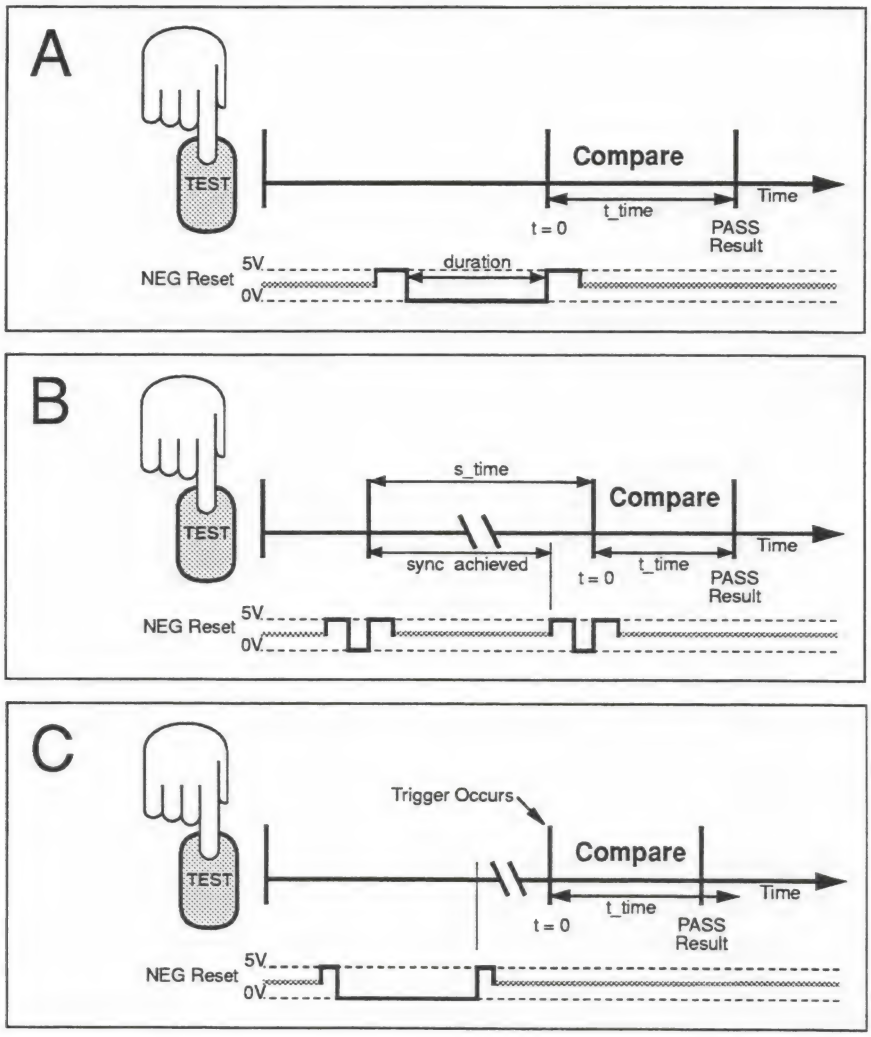



Figure 61

Answers:

| | |
|---|---|
| Synchronous | B |
| Programmable | C |
| Combinatorial | A |

**Condition Checks and Test Cycle**

By default the Clip Test, Float selection will check every pin of the DUT for opens. The test is actually checking for "floating" pins, and thus is actually only checking input pins in most cases. The Float Check is performed at the end of comparison (after t_time has expired), with 10 Kohm pull resistors. All pins that were inactive during t_time, and can be pulled both up and down with a 10 Kohm pull resistor, is considered to be open. The user may turn this test off pin by pin, or entirely for a given DUT.

The Pin_Def menu options permit the user to check any pin for signal conditions: High always, Low always, Active (at least one transition), and the presence of a specified Frequency. High, Low and Active checks are performed for the entire test cycle, including s_time, waiting for trigger, and t_time. During the standard test cycle, a reset pulse is issued and the Frequency measurement taken after the clip test, and before synchronization. Each pin that requires a Frequency Condition Check causes a separate reset pulse and measurement interval.

# SECTION 3
## Test Sequence Development

## 1 Test Sequence Development

A Sequence is a stored set of test parameters for the devices on a circuit board. The parameters are selected while testing these devices on a known-good board; the parameter sets or device tests are stored using the reference designator of the devices as the name. Test may be arranged in an order that represents a logical troubleshooting sequence. After a quick tutorial on Sequence creation, this section examines each test parameter and considers when and how it might be used to make a good device pass during Sequence development.

A Sequence complements the skill of a user by providing a standard troubleshooting order complete with helpful prompts. It also allows the user to jump out of the prescribed order if he wants to verify his reasoned deduction about where the fault is. Sequence development can be done in two ways;

- The New_Seq mode of the tester records the keystrokes and parameter changes as a good board is verified. It creates files that can be enhanced with the keypad Editor with operator prompts and other effects and then stored on a cartridge.

- The 900 PC Software is a Sequence development and tester control environment that permits a PC to act as a development station. Full control of parameters, prompts and test order is possible through a system of popup windows and pulldown menus. A finished Sequence may be downloaded to the tester for storage in cartridge or system RAM and stand alone operation.

# 2 New_Seq Mode Sequence Creation

To reduce the time required for sequence development, the UUT is usually examined to determine which devices are available in the Simulation Library. A Library for that UUT is created and downloaded to the 900 that has the required device library descriptions, and sequence development is begun utilizing the new library.

A simple two device Sequence will be created to show the procedure. Under actual conditions, you would verify that each device passes on a good board and change any parameters as required. For this exercise no parameters will be changed. The following flow diagram shows the four iterative steps and the keystrokes used to accomplish them.

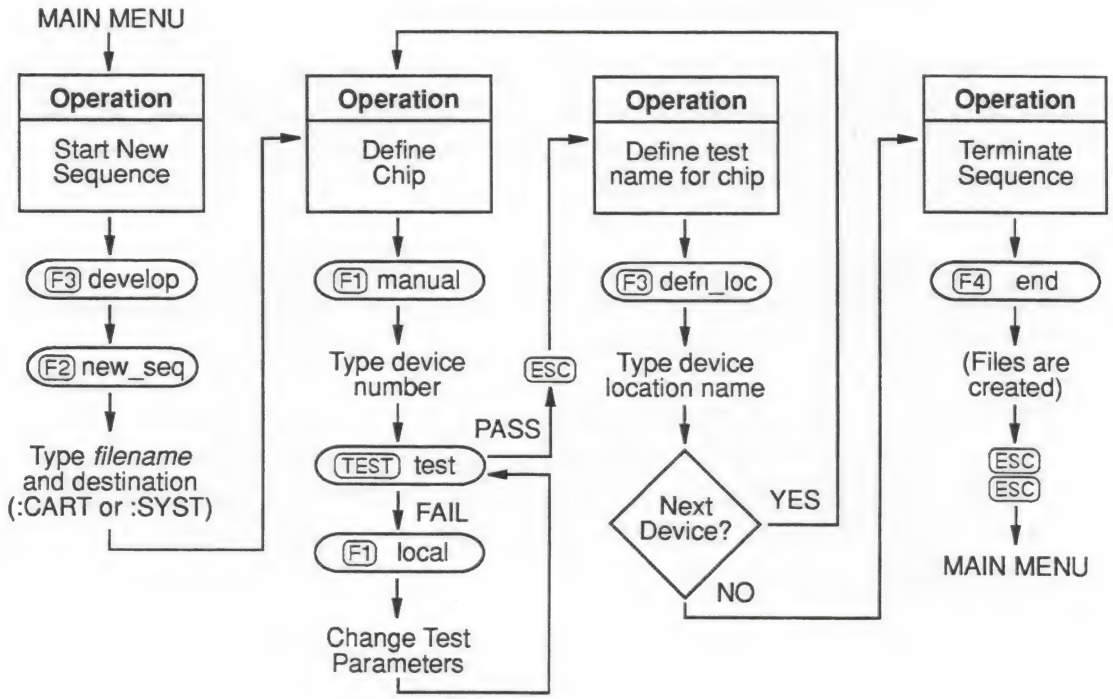



Figure 62

Proceed with the keystrokes shown in figure 62 to start a new Sequence, called TEST1, residing in System RAM. From the Main screen press F3 (develop), F2 (new_seq), T, E, S, T, 1, F5 (:SYST), ENTER.


Figure 63

We will not set a global test parameter, so you may define the first device by pressing [F1] (manual), and loading the device library description for the first hypothetical device, a 74244 for example. Press [7], [4], [2], [4], [4], [ENTER].

Verification on a good board and the changing of parameters to give a PASS result would normally follow. For the purpose of this exercise, assume that the test passes at default settings, and there are no changes required. Press [ESC] to bring up the following screen:

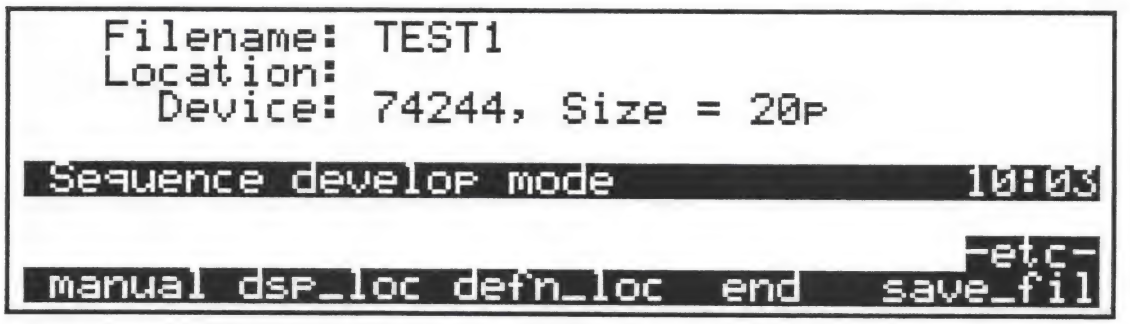



Figure 64

Press [F3] (defn_loc), and [U], [1], [ENTER] to define the location of the 74244 as U1.

Two key labels are not shown in the flow chart of figure 60, but are shown on the Menu Tree listing. One is "dsp_loc", a short form of "display locations". You may press this at any time to examine the device locations defined so far in your Sequence. The locations are ordered left to right, line by line on the screen and may be scrolled with the cursor control keys. [ESC] returns to the previous screen.

The other key label is "save_fil". This key performs a quick storage of your current temporary file to the destination you chose when you named it (System or Cartridge). Normally this would be the cartridge, and by frequently saving your work in progress, you will have a backup copy if you are interrupted by a power loss.

Proceed to add a second device to the Sequence. Press (F1) (manual) and load the device library description for a 7474. Press (7), (4), (7), (4), (ENTER). Again assume for the purpose of this exercise that it passes with the default settings, and does not require any changes to the test parameters. Define its location as U2: (ESC), (F3) (defn_loc), (U), (2), (ENTER).

Up to this point, you have created a temporary Sequence file in the tester's working memory. You could also have stored a backup copy if you pressed the "save_fil" key. The file contains two devices in the order they were entered, with the necessary parameter changes to make them pass on a good board. Press (F4) (end) to terminate this initial Sequence creation. Notice the automatic generation of Sequence source and compiled files.

If you were in the process of creating a lengthy test sequence on a large board, you could either press (F4) (end) or (F5) (save_fil) to store the test, then turn off the system for the night. The next day you could resume where you stopped by using the procedure described above for creating a new test sequence, taking care to use the same name as before. The 900 will re-open the file created the previous day that has the extension .nsq, and warn you that the file exists. You may then proceed as before, from where you left off.

The only problem that this can create is when either of the source files .SEQ or .LOC, has been edited to add user information messages. Each time (F3) (end) is selected from the new_seq mode it will create fresh source and compiled files, overwriting any existing files of the same name. A warning will be given before this happens, but your choices at that moment are to abort (and lose any changes to the .nsq file that you just made), or to overwrite the source files .SEQ and .LOC (and lose the edits that you made to them earlier). It is best to complete the test development in new_seq mode prior to editing the source files to add operator messages.

# 3 Sequence Enhancement with the Editor

The next step in refining a Sequence is to add operator prompts and reorder the tests for convenience in troubleshooting. This typically involves editing the Sequence source file and recompiling it so the tester can execute it. To examine your newly created Sequence source file, press [F1] (files), [F2] (edit), [T], [E], [S], [T], [1], [F3] (.type), [F1] (.SEQ), [F5] ( :SYST), [ENTER].


Figure 65

The functions of the keys for changing editing are explained in the 900 Operator Manual Section 6.7. In addition, Section 5.5 of the 900 Operator Manual describes syntax rules and special commands for advanced users. For example, an advanced Sequence may be edited to include conditional jumps. The effect is to reorder the Sequence flow based on the test results observed while testing.

In the exercise that follows, you will add an operator prompt to the U2 test screen. Notice that your file, TEST1.SEQ, follows certain syntax rules:

- Each line is a command. Blank lines have no effect, but make the listing more readable.
- The colon,":", is used to terminate each command or group of commands. For a .SEQ file, this means that every line that requires operator action (i.e. pressing [TEST]) ends with ":", and for a .LOC file, every group of commands associated with a device ends with a ":".
- One or more spaces are used as field separators. The Tab key is often used to produce readable spacing.
- All commands are indented. Column 1 is reserved for line labels that are used in advanced Sequence programming.

Press [F1] (ins/rev). This allows insertion of a new line (versus revision of an existing line). Press the down arrow key once to position the cursor at U1 and press [ENTER].

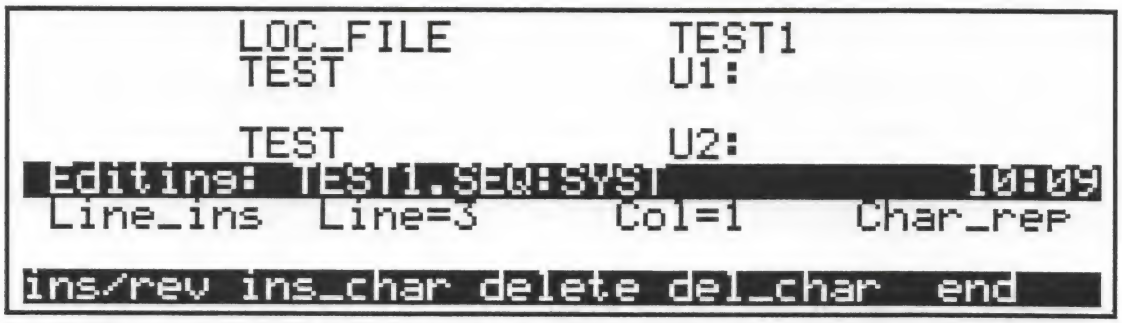



Figure 66

Using the arrow keys, move the cursor out to the colon right after U1. Press [F4] (del_char) to remove the colon. Do not press [F3] (delete), or the entire line will be deleted. Move the cursor to the blank line below U1, and use the [⇆] (tab) key for spacing from the margin. Type in the word DISPLAY, space, followed by a message within quotation marks. End with a colon. Your file should look similar to the picture below.

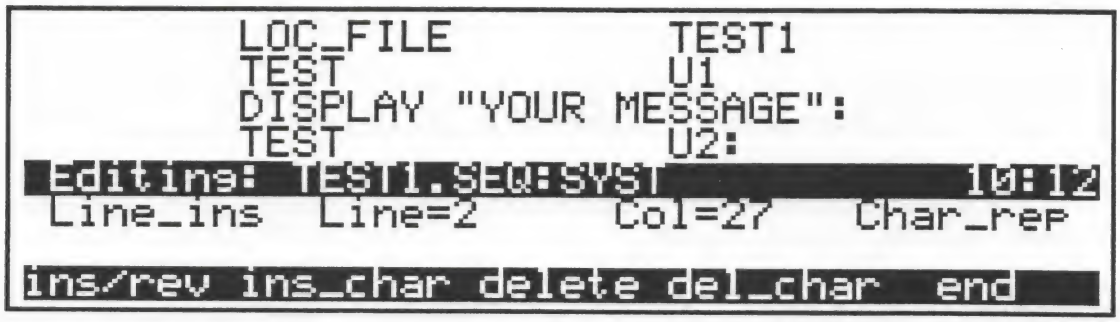



Figure 67

Now press [F5] (end) to save the changes and leave the Editor. Compile the file by pressing [F3] (compile), and typing TEST1.SEQ:SYST. Press [T], [E], [S], [T], [1], [F3] (.type), [F1] (.SEQ), [F5] (:SYST), [ENTER].

You may run the TEST1 Sequence to verify that the operator prompt appears with U1. Go to the main screen, select Sequence Mode and specify your file name. Press [ESC] twice, [F2] (sequence), [F1] (run_seq), [T], [E], [S], [T], [1], [F5] (:SYST), [ENTER].

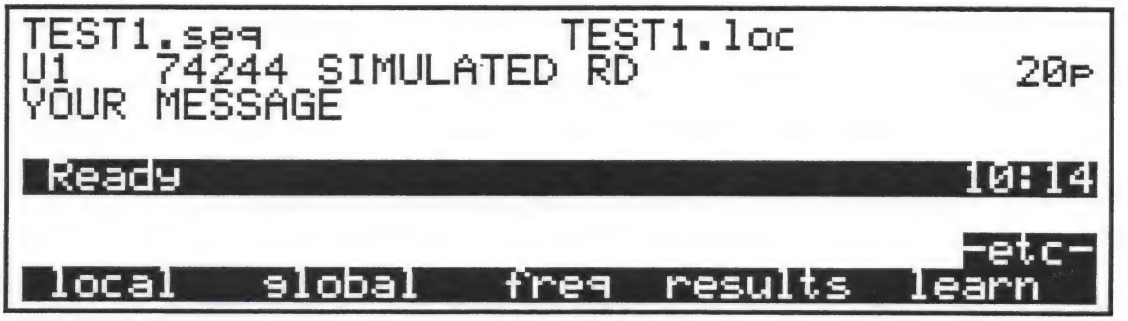



Figure 68

Note the new message on line three of the display. You may place messages on any or all of the first four lines of the display.

Press [ESC], [F5] (yes), [ESC] to return to the main menu.

# 4 Sequence Creation on a PC

### Sequence Creation using the 900 PC Software

Refer to the 900 PC Software Operating Instructions, Section 2, Getting Started, for a tutorial on creating a Sequence on a PC using the 900 PC Software.

The 900 PC Software is commonly used to develop test sequences using the convenience of the larger screen, and standard keyboard of the PC. Once developed, these test sequences may then be used on the PC, or compiled and downloaded using the 900 PC Software menus for stand-alone 900 operation.

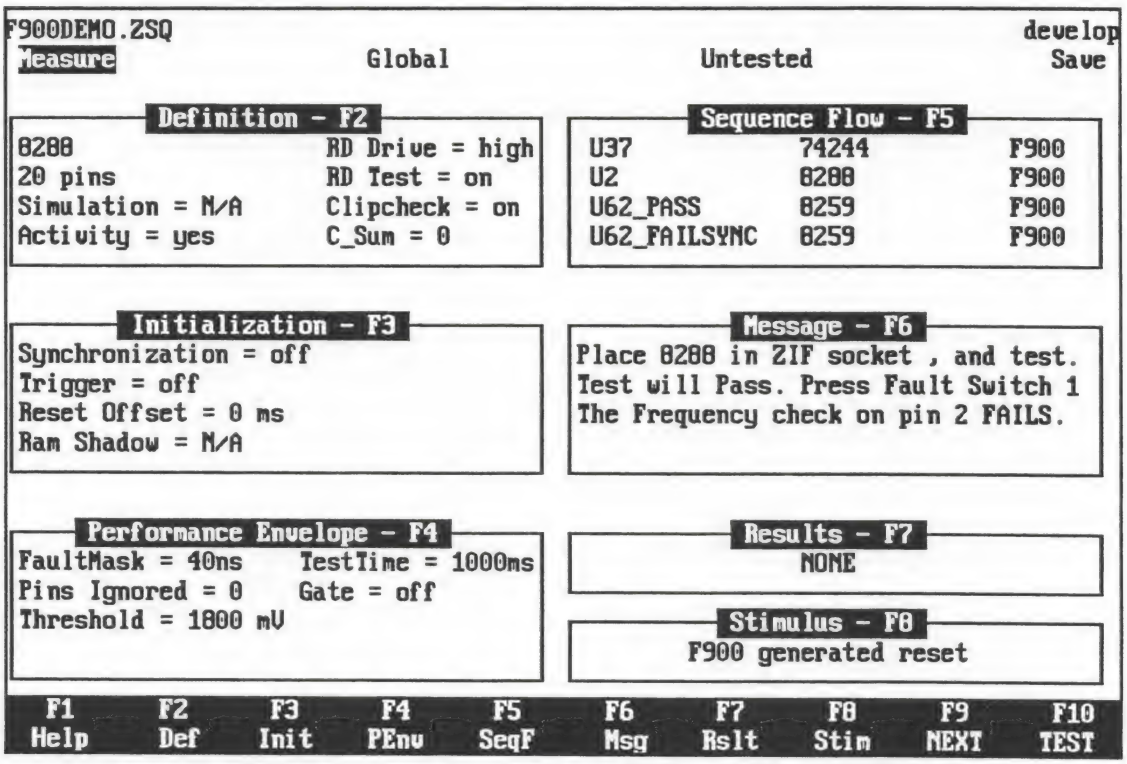



Figure 69

Almost all operations possible from the stand-alone 900 may be performed from the 900 PC Software.

### Sequence Creation using PC Wordprocessing and Communications programs

All of the 900 source files (.SEQ, .LOC, .LIB) may also be created using any ASCII file editor on the PC. It is important to note that most common editors available on the PC will store files in a "word-processor" format that includes special text formatting codes.

These special codes will cause compile errors on the 900. Check the operator manual for that editor to find out how to store the file in "Text" or "ASCII" format.

A simple test to determine how files are stored is to use the DOS "TYPE" command to display the contents of a disk file to the screen. An example of how this command would be used on the file named "AUTOEXEC.BAT" is shown:

C:>TYPE AUTOEXEC.BAT

If the contents of the file are fully legible, with no characters other than standard alpha-numeric characters, then it should be acceptable to the 900 compiler.

To prepare the 900 to receive the file, from the main menu press [F3] (develop), [F1] (files), [ETC], [F2] (dnload).

The 900 prompts for a file name that the received file will be stored as. The filename TEST.SEQ:CART will be used in this example. Press [T], [E], [S], [T], [F3] (.type), [F1] (.SEQ), [F4] (:CART), [ENTER].

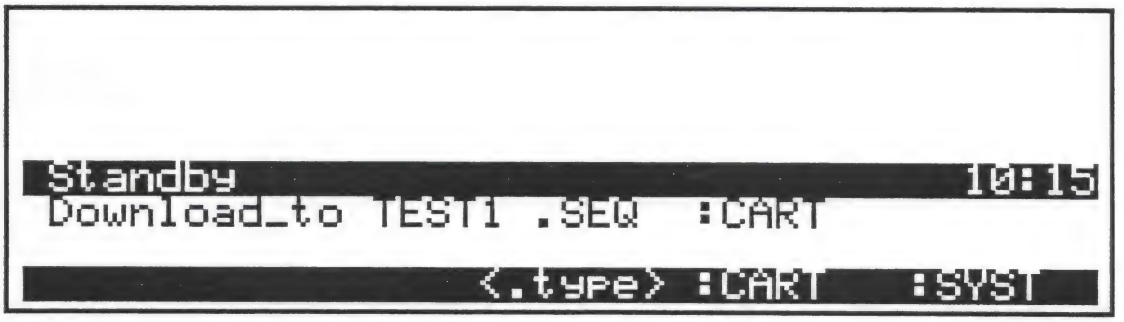



Figure 70

The 900 will take any data received at the RS232 port and store it in the file TEST.SEQ:CART.

Once the file is prepared, use any communications program (such as PCTalk, SmartTerm, etc.) on the PC to transmit the file to the 900 at the correct communications settings. Refer to the 900 Operator Manual, Section 1.6 for information on how to change the 900 communications port settings.

If the end-of-file marker does not terminate receipt of the file, press [ESC] to force termination. The file may now be viewed using the 900 editor, or compiled using the 900 compiler. Once compiled, the file may be executed.

File upload is done in a similar manner using the [F1] (upload) key and a communications program on the PC.

# SECTION 4
## Test Parameters

## 1 Setting Test Parameters

*The following exercises describe how and when to change the 900's parameters. They are not sequential, and may be completed in any order. If you are unfamiliar with the 900, however, and want to improve your overall understanding, it would be best to follow the order of this section.*

*Each parameter is defined, illustrated with a hands-on exercise, and concluded with a concept summary. They appear in the following order:*

Global DUT parameters

| | |
|---|---|
| Local DUT Parameters: | Size |
| | Reset |
| | Test Time |
| | Fault Mask |
| | Threshold |
| | Sync Time |
| | Trigger |
| | Gate |
| | Pin Definition |
| RD Parameters: | RD Test |
| | RD Drive |
| | Simulation |
| | Shadow |
| Clip Parameters: | Clip Check |
| | Float Check |

The test parameter menu options are found under the Manual key which appears in both Manual Mode and Develop Mode. Each parameter will be illustrated in Manual Mode although the same menu is available under the Develop Mode that is used to create Sequences.

The main powerup screen has four function key labels on the bottom of the screen that refer to the four major modes of the 900.

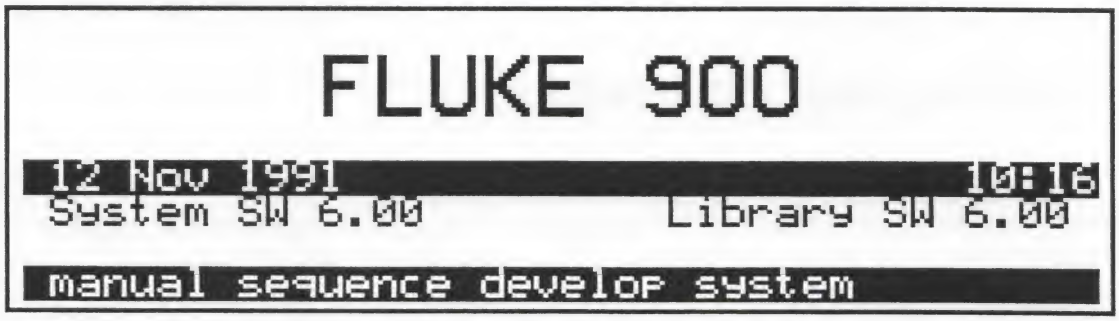



Figure 71

**manual** An immediate mode for testing a single device with its number and test parameters to be entered by the user.

**sequence** A mode for troubleshooting a board using preprogrammed prompts.

**develop** A mode for creating new Sequences and using file utilities (i.e. copy, edit,...).

**system** A mode for setting the 900's option configuration (i.e. serial port, time,...).

There is a hierarchy of sublevels below each key.

(ESC) returns up the menu tree to a previous key level.
(ETC) displays additional labels that are present on a current key level.

Press (F1) (manual) from the main powerup screen to bring up the display shown below. This manual level is assumed to be the starting point for each of the parameter exercises that follow.


Figure 72

The menu tree for the parameters that are examined in this section is shown below:

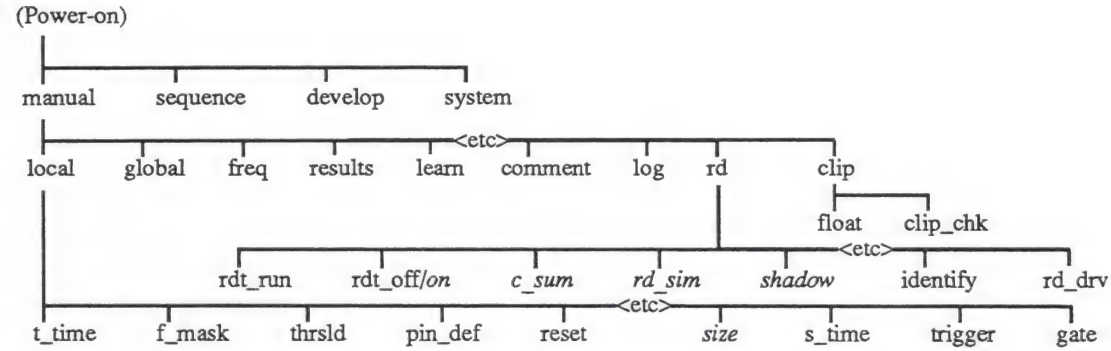



Figure 73

The data cartridge supplied with this course contains simulation files that define the devices used in the following exercises. If the cartridge is inserted into the 900, device simulation will be available as specified in this text. If the cartridge is not inserted, then physical Reference Devices will be required for testing. A physical Reference Device may always be used for testing, even if simulation is available. If simulation is active it can be disabled with the rd_sim parameter.

Ensure that the GND and RST patch leads on the Interface Buffer are attached to the Ground and Reset points of the training UUT (see figure 16).

# 2 Global

Test parameters may be set through either [F1] (local) or [F2] (global). Local means that a parameter only applies to the currently selected IC. Global means it applies to the current IC and all others that follow.

The test parameters found under the global selection are a subset of the test parameters that are found under the local selection. The functions of each parameter will be explained later in this section. The only effect that global has on these parameters is to establish the default (starting) value for each. In most situations they will not be used. Changes to global are only suggested if you find that on a particular board you frequently change a specific parameter.

**Exercise**

Try changing the default (global) setting for one parameter, F_Mask. First note that the default setting displayed on the screen for the F_Mask is 30 ns. Change that default for the current session to 40 ns. Press [F2] (global),[F2] (f_mask), [4], [0], [ENTER], [ESC].

Note that the new default setting for the current session is 40 ns for the parameter F_Mask. If this change had been made while developing a new test sequence, that change would be permanent for that test sequence. Since we are in manual mode, and not in new sequence mode, the default will be restored to 30 ns as soon as we exit the manual mode.

**Test Concept**

Changing the parameters found under the global selection provides a convenient way to establish a board level parameter such as a global Reset, while permitting variations on a per chip basis using the parameters found under the local selection. Usually, global changes are made when a test sequence is first opened, so that the global changes will affect the entire test sequence.

# 3 Size

*The Size parameter specifies the number of pins on a device and its power configuration. It forms part of the library information of a device and specifies how a Reference Device should be powered up in the ZIF socket. It is important to note that when this parameter is changed, many other parameters are returned to default settings.*

*Because the Size parameter provides the ability to test digital devices that are not in any library, it is possibly the most powerful feature of the 900.*

Special attention was given to ensure that the basic design of the 900 allowed for testing of all common digital devices on the market when it was introduced. This largely took the form of placing relays around the ZIF socket to allow power and ground to be routed to the appropriate pins of the RD. The diagram below shows the placement of these relays in the 900. Since the 900 was released, there have been a number of new devices introduced that have different power and ground configurations.

If you have a non-standard device to test that is not in the 900 Library, position it over the diagram below on the left for a quick check to see if there is a configuration of power and ground that will allow for testing of that device.

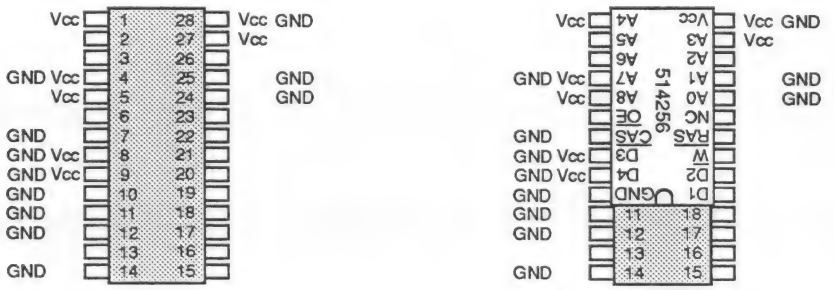



Figure 74

The diagram above on the right shows that the 514256 RAM device found on the self-paced trainer board can be tested if it is placed in the socket (and clipped) backward. To test the 514256 without a device library description you would set Size to 20 pin, standard power and ground configuration. By placing the device in the ZIF socket backward (as shown above), and clipping the DUT in the same manner, you would be ready to change other parameters as necessary. In this case use of a Trigger would be recommended.

**Exercise**

For this exercise, a 7400 device will be tested as if it were not in the Library. From the manual level, press (F1) (local), (ETC).


Figure 75

Press F1 (size), 1, 4, then ENTER on the command line. Notice that the left side of the display now reads: "SIZE 14 STD." STD means standard and refers to the power pin configuration. For a standard 14 pin device, Ground is pin 7 and Vcc is pin 14.

In order to specify a nonstandard device (in our example we will actually use a 7400), enter F1 (size), 1, 4, F2 (NSTD), ENTER. The display now lists the available power pins that you may assign. Press F3 ( Vcc), 1, 4, F4 (Gnd), 7.

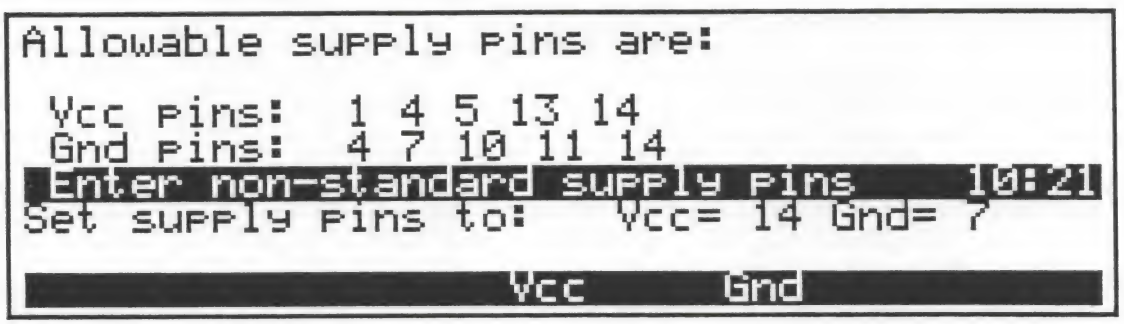



Figure 76

Press ENTER, then test U42 (use U14 on the sales demo trainer), by clipping on it with a Test Clip, inserting a 7400 Reference Device in the ZIF socket and pressing TEST. You may need to use the 16 pin test clip because U42 does not quite line up with the next device, and may prevent proper seating of the clip on U42.

Press ESC to return to the manual menu.

**Test Concept**

The Size parameter is used to test devices that are not resident in the tester's library. Most other parameters are set to system default values when size is set. Normal adjustments to the default parameters may then be required for testing (in the same manner as testing a chip called up from the library.)

# 4 Reset

*Reset defines the attributes of a pulse issued on the patch lead labelled RST and is intended to force a UUT to a known initial state before testing.*

**Exercise**

Various attributes of the Reset parameter will be changed. From the manual level, load the device library definition for a 7400. Press [7], [4], [0], [0], [ENTER].

Press [F1] (local), [F5] (reset).

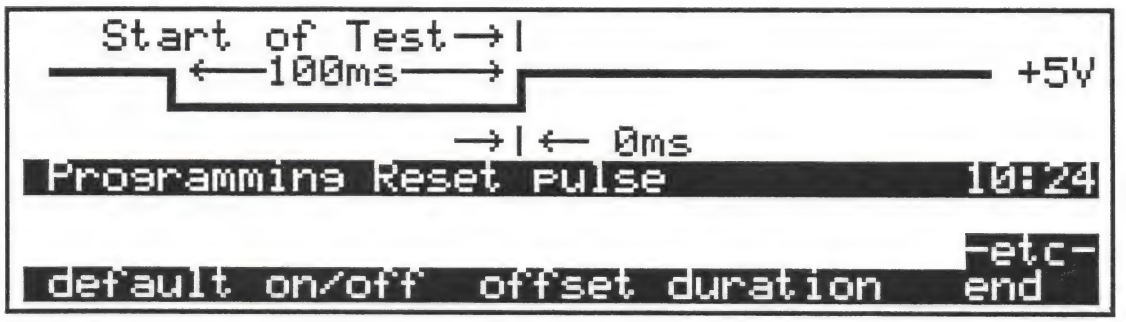



Figure 77

Observe the effect of pressing [F2] (on/off), [ETC], [F2] (polarity), and [F1] (supply). This last key causes the voltage on the Reset lead to be sourced either internally (5 Volts), or from an externally supplied voltage on the VCC patch lead. [F1] (default) returns the Reset setting to its initial setting.

Press [F3] (offset) and enter a negative offset time on the command line. For example, the value -1000 produces the following screen. Press [F3] (offset), [-/], [1], [0], [0], [0], [ENTER].

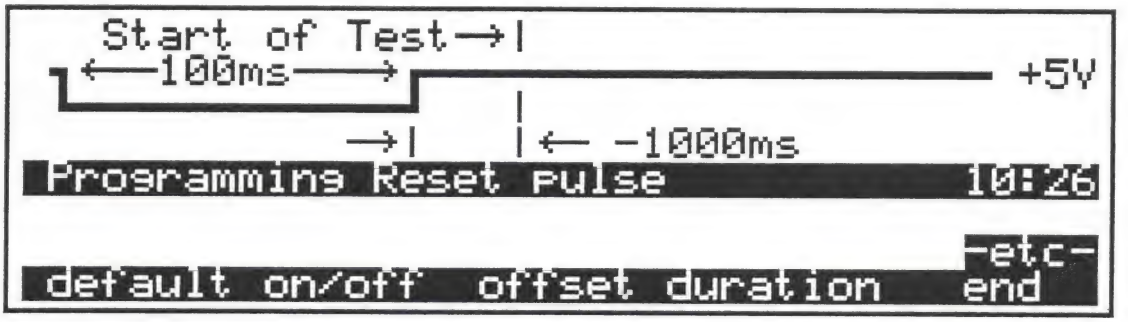



Figure 78

Press [F5] (end) to accept the Reset parameter settings. Clip on the 7400 located at U42

(use U14 on the sales demo trainer), insert a 7400 Reference Device in the ZIF socket if it is not simulated, and press (TEST). Notice that on the Status Line of the display,"Waiting to start test" appears momentarily. The offset has shifted the start of comparison relative to the Reset pulse issued to the board.

Offset is one way to wait for on-board activity to initialize a programmable device before comparing DUT and RD. It is not recommended that test sequences include a reset offset for programmable type devices. For programmable devices use of the test parameter Trigger is recommended as a more reliable method to start the test. If the DUT were not initialized properly, the message "Waiting for trigger . . ." would indicate that fact.

**Test Concept**

The Reset pulse is used as a board level synchronization technique to force the UUT to a known state and make the stimulus repeatable. For locked up or "dead" boards, a reset pulse causes a burst of activity which is used by the 900 to isolate the fault.

# 5 Test Time

*Test Time (t_time) defines the length of time that the DUT will be compared to the RD before a pass result is given.*

**Exercise**

Change T_Time to continuous and check for an intermittent fault.

From the manual level load the device library description for a 7400, press (7), (4), (0), (0), (ENTER) if it is not already loaded. Press (F1) (local), (F1) (t_time).

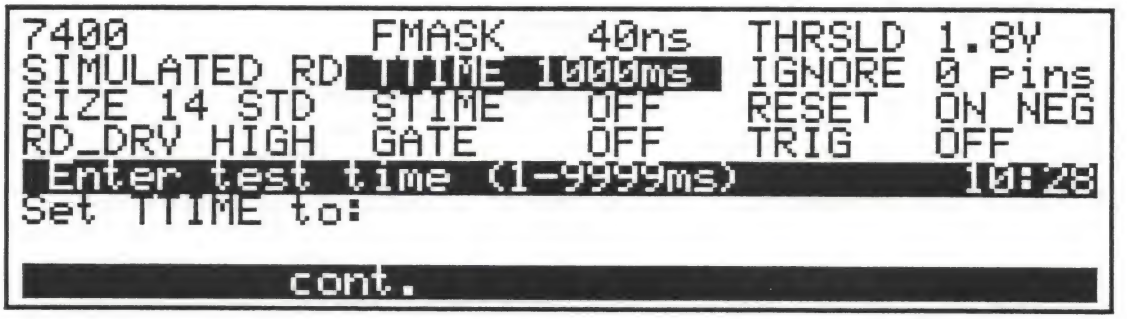



Figure 79

Press (F2) (cont.), (ENTER) to set the value to continuous. Clip on the 7400 located at U42 (use U14 on the sales demo trainer), insert a 7400 Reference Device in the ZIF socket if it is not simulated, and press (TEST). The testing will last until you press (TEST) again, or until a fault is captured. For example, while the 900 is continuously testing U42, use a spare patch lead to ground an output on the DUT (e.g. pin 1). In actual troubleshooting you could apply a heat gun or freeze spray while continuously testing to see if a fault appears.

Press (ESC) to return to the manual menu.

**Test Concept**

Test Time should be set to the duration of the stimulus on the board under test. When developing a Sequence, it is often convenient to use a continuous test time and manually terminate each test until you have a good idea of the length of the stimulus.

# 6 Fault Mask

*Fault Mask or F_Mask defines how close to compare the output signals of DUT and RD.*

**Exercise**

Adjust F_Mask to make a DUT pass when it experiences normal loading in its circuit. From the manual level enter the IC number 74244. Insert a 74244 in the ZIF socket if it is not simulated, clip on U79 (use U37 on the sales demo trainer), and press [TEST].

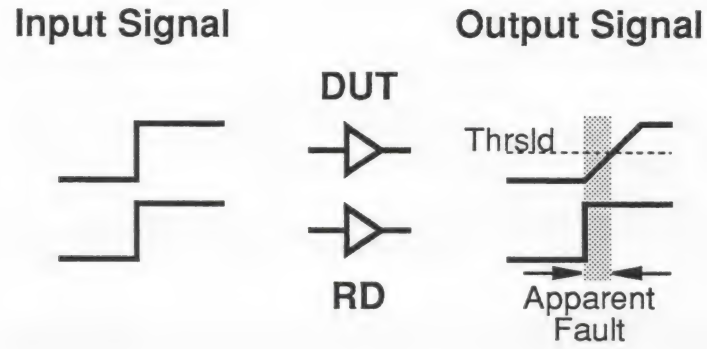



Figure 80

The FAIL test result on this good DUT indicates that F_Mask should be increased to account for in-circuit loading of the DUT. Press [ESC] to leave the fail screen, and note that F_Mask is 30 ns by default (40 ns if the global change made earlier is still in effect).

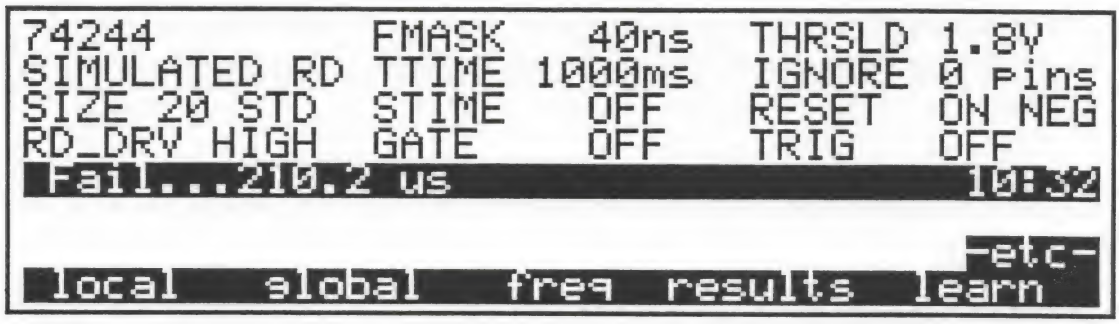



Figure 81

Press [F1] (local), [F2] (f_mask), and enter a larger F_Mask value. Repeat this process until you obtain a PASS test result.

As an alternative, 900 firmware version 6.00 and higher supports a key labeled Learn that is found under [F5] (learn) of the manual menu. You may need to press [ESC] to return

to the manual menu. Use of the learn key will provide test results for thirty-six combinations of F_Mask and Threshold. To try Learn, press [F5] (learn), [F2] (execute).

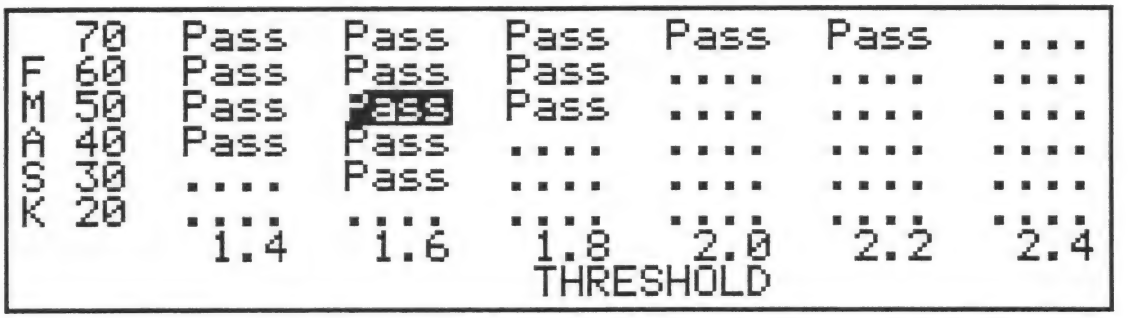



Figure 82

Once you have test results for the whole matrix. Press [ESC] once, then [F5] (end) to store the recommended settings, which are indicated by the highlighted combination (see figure 82). If [F5] (end) is not selected, the suggested settings will not be stored. Depending on the test results, there may be a key labeled 'advice' present on [F4] (advice) after the test has run. This selection will suggest alternate parameter changes that may improve the test, or other information that the technician should know about the preceding Learn. If no highlighted pair of parameters is suggested, the 900 Learn algorithm did not have sufficient Pass results to select a suggested setting. Consult the [F4] (advice) selection if no pair of parameters was suggested.

Special note: On boards with fast signals, some care must be taken to avoid setting values for F_Mask that are longer than the fastest signal pulse width of the DUT. Refer to the next section on Threshold that discusses how to make Frequency measurements. The F_Mask setting should never be larger than the smallest value of time high or time low, as measured on the DUT using the Frequency measurement. If F_Mask is set to a larger value, a pin could be failing comparison, but it would not be detected as failing because the signal on that pin was masked out.

Press [F5] (end) to store the recommended settings and return to the manual menu, and [TEST] to verify the new "learned" settings.

**Test Concept**

When F_Mask is increased to make a DUT pass on a good board, it is recommended to add an extra 10 ns to the final value. This will allow for a possible range of good boards. When first testing with a new Sequence, a few small adjustments may have to be made to F_Mask settings to account for normal IC loading variations. If the Learn key is used to determine settings for the F_Mask parameter, a 10 ns safety range will be included in the suggested settings. However, special care must be given to setting the F_Mask parameter on fast boards.

# 7 Threshold

*Threshold defines the voltage level, above which the 900 registers the logic state at a pin of the DUT as logic 1 and below which is logic 0. This threshold voltage level may be varied for the DUT, but not for the RD.*

**Exercise**

Observe the duty cycle of a signal when it is acquired with two different Threshold settings.

From the manual menu load the device library description for an 8284, press [8], [2], [8], [4], [ENTER]. Note that the threshold is 1.8 V by default. Clip on U11 (use U91 on the sales demo trainer), which is a 8284 oscillator chip. Press [F3] (freq), [2], [F5] (detail), [ENTER].

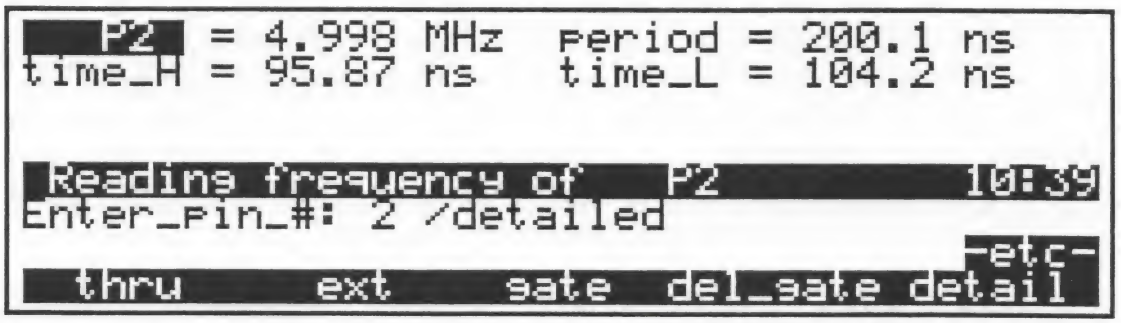



Figure 83

Note the time high(time_H) value, then press [ESC] to exit Frequency mode.

Change the Threshold to 3 V by pressing [F1] (local), [F3] (thrsld), [3], [ENTER]. Press [ESC] to return to the manual level and use the Frequency function to monitor pin 2 as before. The time high value should be different this time because the signal has rise and fall times as shown in the diagram below.

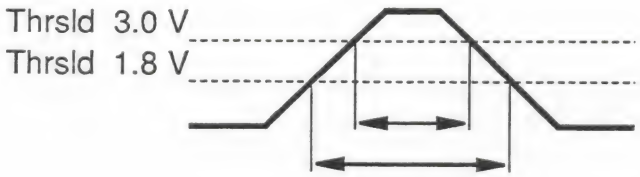



Figure 84

Use of the Learn key described above with the F_Mask parameter can also be very helpful

when trying to select an appropriate setting for Threshold.

Special note: In the previous section on F_Mask it was noted that care should be given to how large a value of F_Mask is used. In the frequency measurement above, if an F_Mask setting of 100 ns or larger was used, pin 2 would never fail. Each time the signal on pin 2 transitioned, the signal would be masked out for the value of F_Mask. In this example, since the signal transitioned again before F_Mask had expired, the count would be restarted on that pin without comparison ever having taken place while it was high.

**Test Concept**

Although Threshold is a voltage parameter, it has an effect on signal timing by shifting the apparent edges of signals. The mid-range default Threshold value is usually the best setting. Occasionally, especially for clocked devices, changing Threshold can be used to shift a signal and overcome a "race" problem that puts DUT and RD out of phase. (See also Section 2, part 3.3.1, "Timing Race on Synchronous Devices.")

# 8 Performance Envelope

*The test parameters that affect the comparison portion of DRC testing define the Performance Envelope of a DUT. Such parameters include Test Time, Fault Mask, Threshold and Gate. Other parameters have more to do with defining and synchronizing a device.*

A change in the Threshold setting for a device will often have an effect on the required F_Mask. This is especially true when the input signals to a device are loaded and have longer rise and fall times. For example, in the diagram below, a buffer is shown with a slow (loaded) signal on the DUT input and a fast (very little loading) signal on its output. F_Mask accounts for the apparent output timing mismatch between DUT and RD. Lowering the Threshold causes the RD behave more like the DUT and results in a lower required F_Mask. Note that the F_Mask parameter applies only to output pins, while the Threshold parameter affects both inputs and outputs.

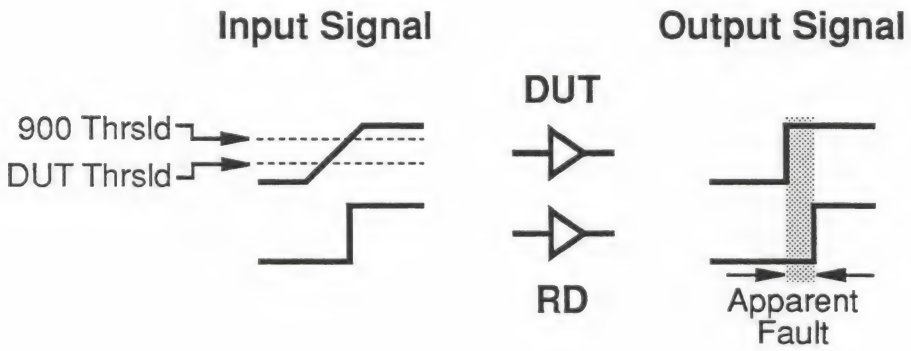



Figure 85

The recommended procedure when establishing the Performance Envelope for a device is to leave Threshold at a mid-range setting and vary F_Mask within reasonable limits to account for output loading. If increasing F_Mask by about 80 ns does not make a DUT pass, there is reason to suspect some other problem. Varying Threshold accounts for input signal loading and also for "race" problems on synchronous clocked devices. The Gate parameter described later accounts for contention problems on bus devices that may appear to be a loading problem.

# 9 Sync Time

*Synchronization Time or S_Time defines the maximum time that the tester will try to synchronize the DUT and RD to the same state before comparison testing.*

**Exercise**

Test a 7474 Flip Flop with, and without S_Time enabled to observe the 900's synchronizing techniques.

From the manual level load the device library description for a 7474. Insert a 7474 in the ZIF socket if it is not simulated, and clip on U10 (use U11 on the sales demo trainer). The clear pin of this Flip Flop is connected to the board reset so disconnect the RST patch lead from the board to make it a free running circuit. Press [TEST]. Note that the word "Synchronizing ..." appears momentarily on the Status Line at the beginning of the test.

This interval is used to put the DUT and RD into the same state before testing. If you time the duration that the word "Synchronizing ..." appears on the status line of the display, you will find that it is less than the 3000 ms (three seconds) permitted. As soon as synchronization is achieved, the 900 immediately starts the comparison test.

Turn to the Test Cycle description in Section 2, and Library creation in Section 4 for details on the specific synchronizing techniques employed.


Figure 86

S_Time information resides in the library description for the selected device. Synchronizing information is normally only changed by the user for devices not in the library, or for PAL devices. Note that for the 7474, S_Time is set to 3000 ms. Disable S_Time to show the effect on testing. Press [F1] (local), [ETC], [F2] (s_time), [F2] (off), [ENTER], [TEST].

With RST still disconnected, test U10 again. The failure of multiple outputs or different failed pins for each test is a common symptom of a synchronization problem.

Reconnect the RST patch lead before proceeding to the next exercises. Press [ESC] twice to return to the manual menu.

**Test Concept**

Sync Time takes place prior to the actual comparison testing, and lasts only as long as necessary to synchronize DUT and RD. It should be set to a large enough value for on-board activity to appear and assist the synchronizing process. 3000 ms, which is the default value, is the recommended minimum.

# 10 Trigger

*Trigger defines logic states on the DUT pins and EXT which, when they occur, initiate the start of comparison testing.*

**Exercise**

A simple External Trigger will be used to synchronize a device test to an asynchronous event. To start this exercise, the EXT patch lead should not be connected to the board.

From the manual level load the device library description for a 7432. Insert a 7432 Reference Device in the ZIF socket if it is not simulated, and clip on U16 (use a 7400 device at location U14 if you have the sales demo trainer). The EXT lead on the Input Buffer has a pull-up resistor on it like the other 28 input channels of the test clip so that when the EXT lead is unconnected, it is pulled to a logic 1.

Set the Trigger to detect a logic 0 on the EXT lead. Press [F1] (local), [ETC], [F3] (trigger).

Move the flashing cursor to the "x" on the far right by pressing the arrow keys. Press [0].

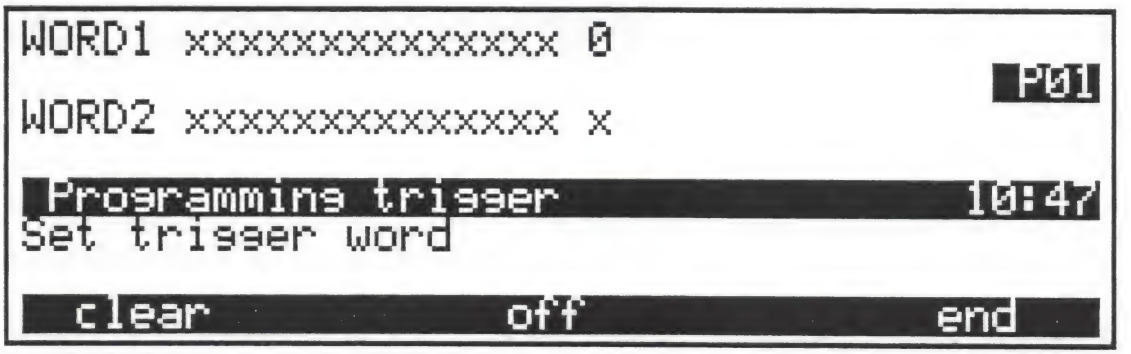



Figure 87

Press [F5] (end) to confirm the setting. Test U16 and notice that the 900 waits indefinitely for the appearance of the Trigger.

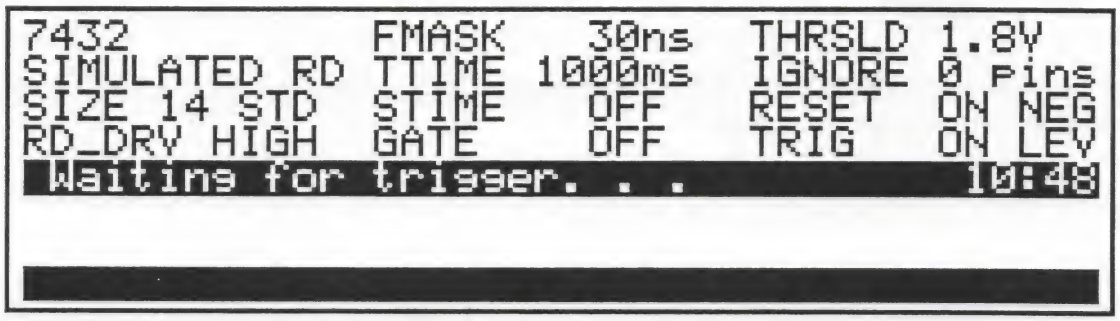



Figure 88

You may press (TEST) again to stop the test.

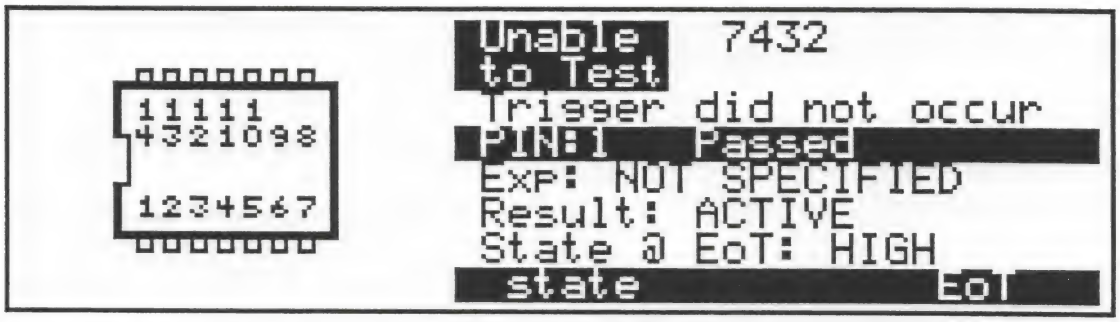



Figure 89

Press (ESC) to leave the fail screen.

Test U16 again. This time while waiting for Trigger momentarily ground the EXT lead to initiate comparison testing.

Press (ESC) to return to the manual menu.

**Test Concept**

Trigger can be used to ensure initialization of a complex device as shown in Section 2, part 3.4, for a 8259 Interrupt Controller. The External Trigger used in the exercise just completed usually serves to synchronize the tester to some signal on the board. External Trigger can be used as an alternative to the Reset lead when the UUT cannot be reset by the 900 (such as when the board being tested is a peripheral card to a larger system that is running diagnostics).

# 11 Gate

*The Gate word defines a condition on the DUT and EXT which, when it appears, causes comparison testing to be enabled until that condition disappears. It may be thought of as defining a window of valid testing within the Test Time.*

**Exercise 1**

A parity generator chip will be tested using External Gate attached to various signals.

From manual level, load the device library description for a 74280, press [7], [4], [2], [8], [0], [ENTER]. To avoid confusing test results, there are two additional steps to be taken. First press [ETC], [F4] (clip), [F1] (float), [F4] (all/none), [F5] (end), [ESC], and [ETC]. Second, temporarily remove the shorting plug at JP10 (near the GND and RST connections).

Insert a 74280 Reference Device into the ZIF socket if it is not simulated, and clip on U51 (use U70 on the sales demo trainer). Press [TEST] and note that a FAIL test result is obtained. Press [ESC] to leave the failure screen.

Enable an External Gate. Press [F1] (local), [ETC], [F4] (gate). Use arrow keys to position the flashing cursor over the "x" on the far right (the EXTernal signal). Press [0].

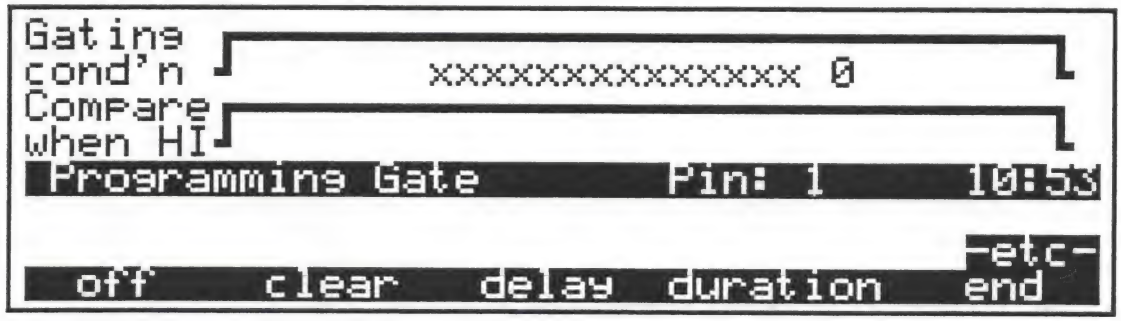



Figure 90

Press [F5] (end) to accept the Gate setting. Open the TTL Databook to the description for a 74LS280 device. Note that it is a combinatorial type device that does not tristate . From the drawing in figure 92, you will see that it receives its inputs from the memory data bus. The outputs of U51 are only valid when its input data is valid. In the following three steps, we will show what happens when the External Gate that we have set is never present, always present and present only when data is valid for U51.

Step 1 Connect the EXT patch lead to a Vcc pin on a convenient device (e.g. pin 16 of U3). Press [TEST].

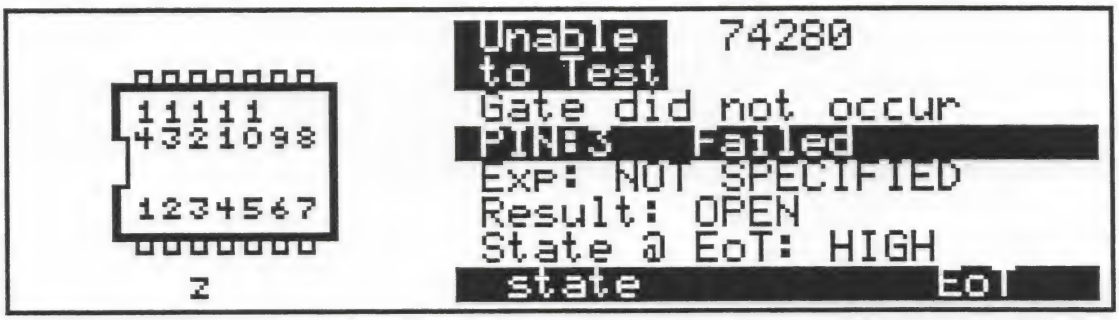



Figure 91

The External Gate, which is set to test when a logic 0 appears on EXT, is never satisfied.

Step 2 Connect the EXT patch lead to a GND pin on a convenient device (e.g. pin 7 of U4). Press (TEST).

The External Gate, when connected to a logic 0, is always satisfied. Therefore, this configuration is the same as not setting a Gate. We obtain a FAIL test result, just as we do when no Gate is set.

Step 3 Connect the EXT patch lead to pin 15 of one the RAM chips (e.g. U70 on the self-paced trainer, or U57 on sales demo trainer ). This is the CAS signal to the RAM, which indicates there are valid address and data signals present. Press (TEST). A PASS result should be obtained.

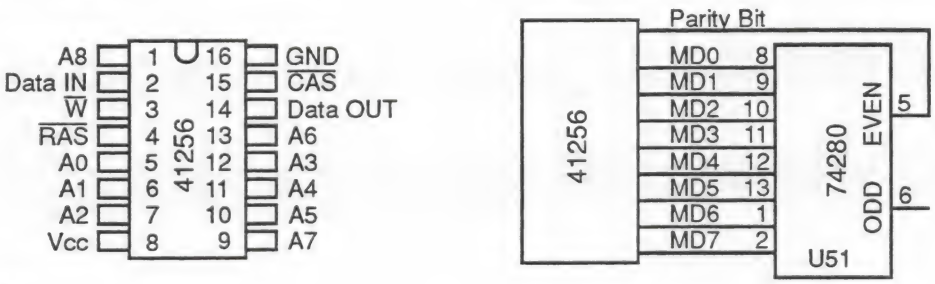



Figure 92

Restore the shorting plug to JP10, and press (ESC) to return to the manual menu before proceeding.

**Exercise 2**

A bus driver will also be tested using a Gate on signals to the DUT pins.

When a tristate device such as a bus driver requires a Gate, it is usually possible to define the setting from the pins on the DUT without resorting to use of the EXT lead. As an

example, we will set a Gate for a 74244 which exhibits bus contention and was tested previously in Section 2.

Load the device library description for a 74244, press (7), (4), (2), (4), (4), (ENTER). Insert a 74244 Reference Device into the ZIF socket if it is not simulated, and clip on U64 (use U43 on the sales demo trainer). If you press (TEST), it will fail. Set a Gate condition on the enabling pins of the DUT:

Press (F1) (local), (ETC), (F4) (gate). Use arrow keys to position the cursor and put 0 on pins 1 and 19 (refer to Section 2, part 3.2.2, for more information on this Gate selection).

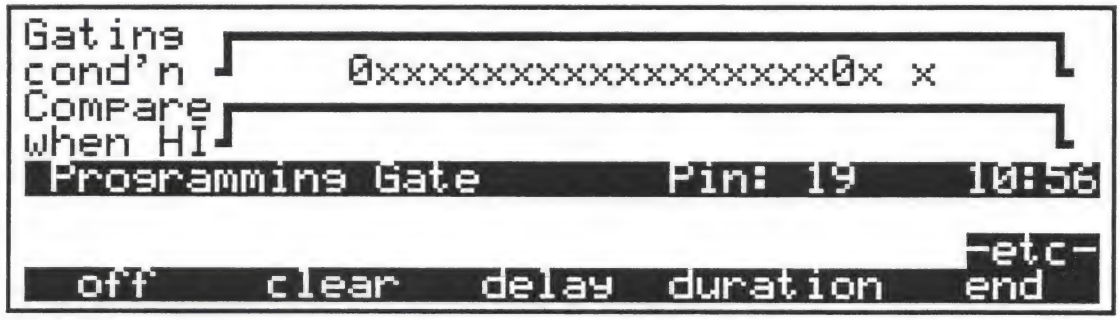



Figure 93

Were you to press (F5) (end) to accept the Gate setting at this point, you would not notice any difference in the test result (it will still FAIL).

The additional parameters necessary for the gate are Delay and Duration to mask out the invalid data present on U64 at the edges of its enabling signals. The smallest value for each of these parameters is 40 ns. Changes to these parameters must be made in increments of 40 ns, or the base value of the current range. Any value typed that is not an increment of the base value of the current range will be rounded to the nearest legal value, (see section 3.3.9 of the Operator Manual for a table of ranges). The process for determining these values is as follows:

First, determine if there is contention at the beginning of the Gate time period. Set Duration to a small value, such as 80 ns: press (F4) (duration), (8), (0), (ENTER), (F5) (end).

> Note: Be sure that when a value for Duration is set, that it is never equal to, or shorter than the current setting for F_Mask. If it were, the entire comparison test may be masked out, leaving the impression that a comparison test took place when in fact it did not.

Press (TEST). If the test fails, Set Delay to 40 ns (its smallest value): press (F3) (delay), (4), (0), (ENTER).

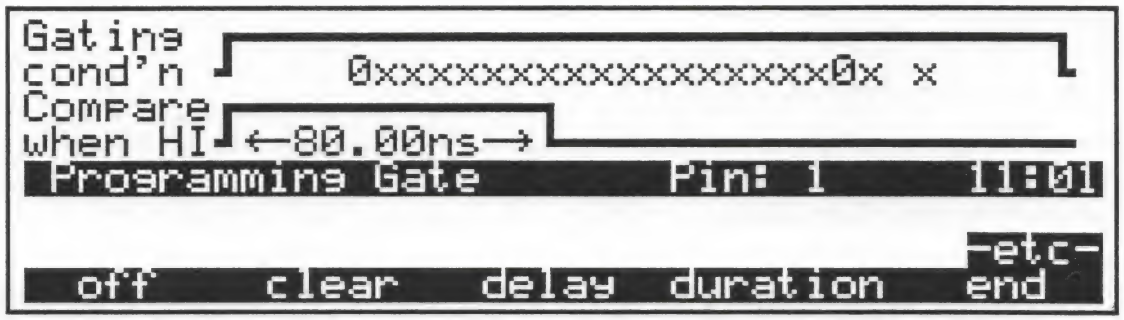



Figure 94

Test U64 again. If it passes, you have the correct Delay setting. If it fails, you must increase the Gate Delay in increments of not less than 40 ns until it passes. Once the test passes, the contention on the leading edge of the Gate is masked.

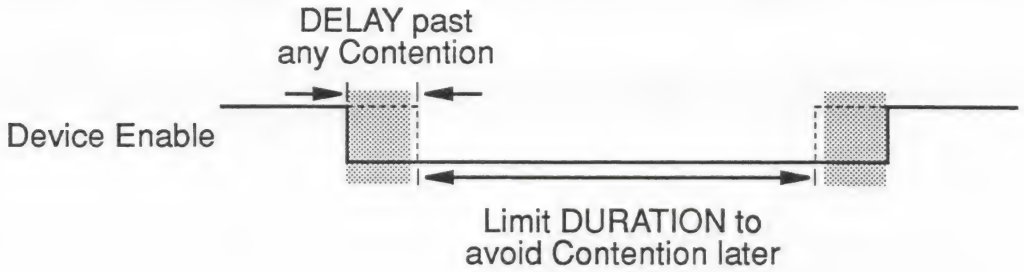



Figure 95

If the test passed, or you now have enough Delay to cause the test to pass, increase the Duration setting until the test fails again, and then decrease it back to where it passes. This means that any contention on the trailing edge of Gate is also masked. A setting that has been found to work on U64 is shown below.

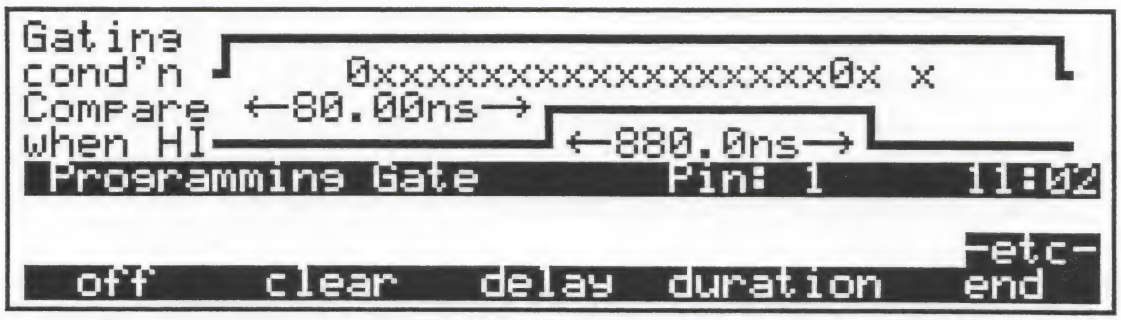



Figure 96

To speed up the process of discovering the correct value for Duration,

it is often useful to know the length of time that the Gate is being met (pins 1 and 19 are both Low). This can be easily done once the Gate word has been set by pressing [ESC] to return to the manual menu, then select [F3] (freq), [F3] (gate), [F5] (detail), [ENTER].

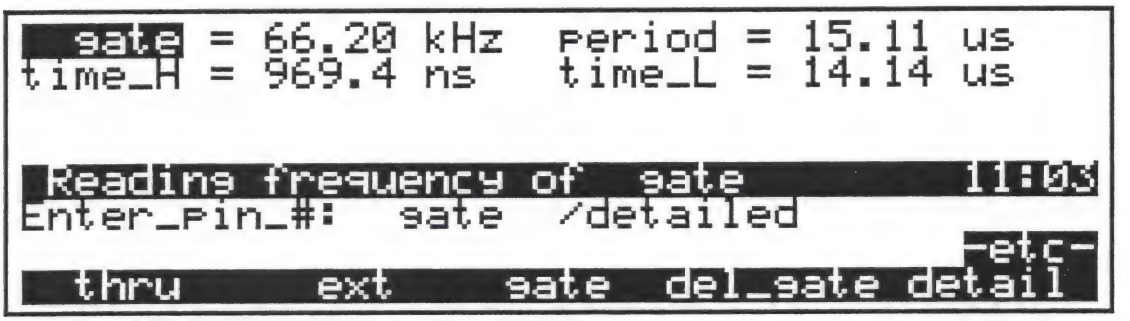



Figure 97

The value shown as time_H represents how long the conditions described by the Gate word are being met (in this case, pin 1 and 19 are simultaneously Low for 969.4 ns). This number also represents the total length of time that can be influenced by the Gate Delay and Duration settings. Delay and Duration added together must not exceed this value. If the sum of the Delay and Duration settings exceed this value, then any remaining Delay and Duration time will be truncated. The timing cycle of Gate is started over each time Gate becomes true.

Press [ESC] to return to the manual menu.

It is good practice, unless there is some reason not to, to use Gate on the enable pin(s) of any device that is capable of tristate conditions — even if an enable pin is tied to Vcc or GND. You may be led to believe that this is not necessary because both the DUT and RD automatically go into a high impedance state when pins 1 and 19 are at logic 1. The 900 senses this while monitoring the RD. As a result, while it does not actually disable comparison temporarily, the net effect is the same since all of the output pins are tristate. In this way, tristate devices have a "natural" Gate that is always present (see also the rd_test description for more information about floating or tristate pins). By setting a Gate condition on pins 1 and 19 of the 74244, we are duplicating what is present for this device even without a Gate setting. The major advantage to setting the Gate parameter is that if the device is never selected, the 900 will notify you that the comparison test never took place. Without the Gate parameter the operator is led to believe that a comparison test took place, when in fact it did not. For this reason a Gate should be used on any device that is capable of tristate.

**Test Concept**

Gate may be thought of as defining windows of valid data within Test Time. It is mainly used on devices that have tristate outputs or that are receiving input signals that can go tristate.

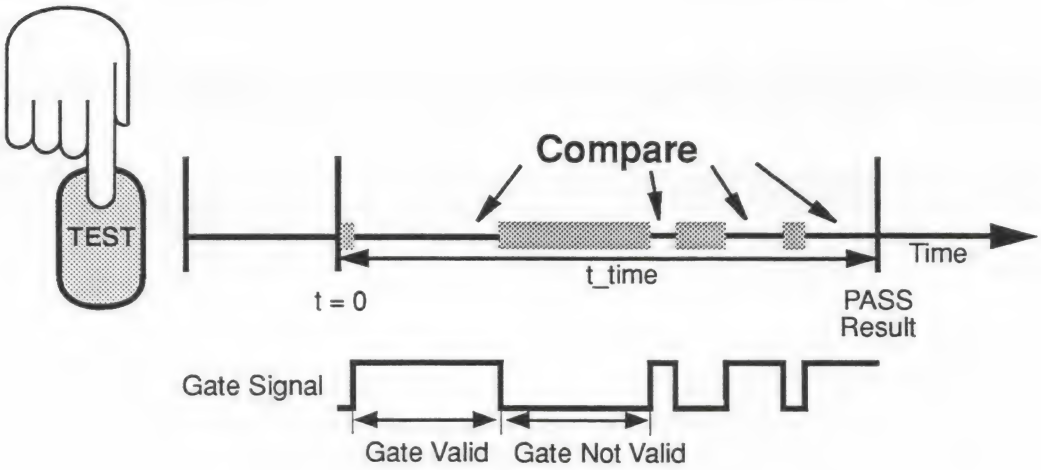



Figure 98

# 12 Pin Definition

*Pin_Def allows the user to disable or re-enable comparison testing on each pin of a device. It also permits Condition checks to be set for each pin to verify high, low and active signals, and specific frequencies.*

It should be noted that on all 28 pins of the test clips and the EXT test lead there is always a 10 Kohm pull-resistor. There will be a 10 Kohm pull-up in all cases except when a condition test for High is present, or the pin is Vcc. In those two instances there will be a 10 Kohm pull-down. This is to ensure that each pin of the DUT is actually driving the signal on that pin, and it is not floating or tristate.

An exception to the effect of the pull-resistors is presented by the Y900-16DZ High Impedance test clip. It contains active buffering components. Due to the active design of this clip, signals will be pulled Low on any pin that is not being driven. If a secondary condition test for Low is assigned, and that pin is actually floating, it will pass the condition test without having been detected as floating because of the pull-resistor in the clip. Additional information about this test clip is packaged with the test clip.

**Exercise**

A device will be tested in two parts using Pin_Def to ignore the other part.

From manual level load the device library description for a 7404, insert a Reference Device in the ZIF socket if it is not simulated, and clip on U25 (use U36 on the sales demo trainer). Press [TEST] to test the device.

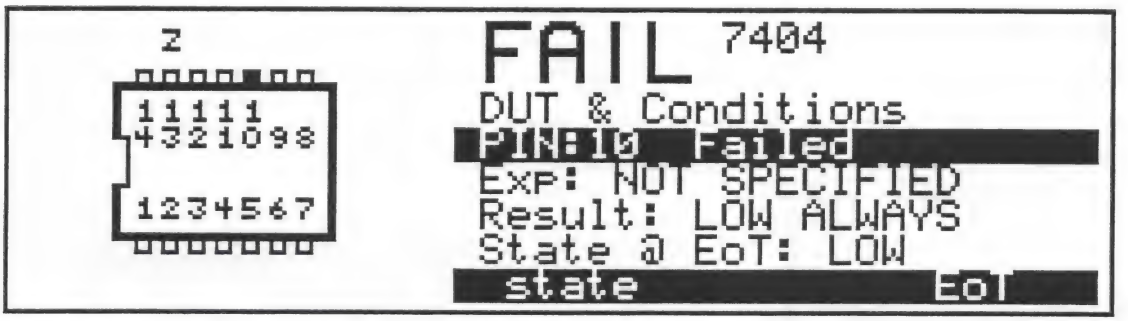



Figure 99

Note that pin 10 fails comparison. Recall that when a pin fails comparison, the corresponding monitor LED will flash. The failure is the result of pin 10 being connected to the base of a transistor, and it cannot rise to TTL logic one level. See figure 100.

On the self-paced trainer pin 13 failed only the floating pin test. On the sales demo trainer

pins 5 and 9 fail only the floating pin test. Note that the only indication of the floating pin condition failure is the "Z" character in the failure screen.

(The diagram below is for U36 on the sales demo trainer. U25 on the self-paced trainer is used similarly, but has only one unused (no-connect (NC)), gate instead of two.)

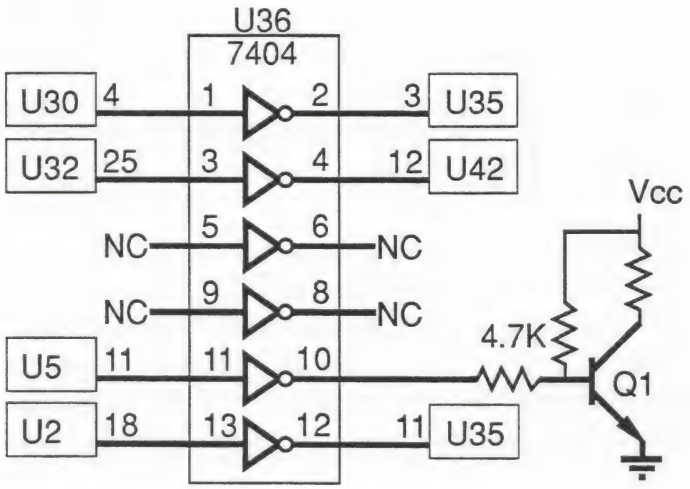



Figure 100

We will first disable the floating pin test, as it does not apply to this exercise. Press [ESC] to leave the fail screen, then [ETC], [F4] (clip), [F1] (float), [F4] (all/none), [F5] (end), [ESC], [ETC].

For this exercise, we will first ignore pin 10. Press [F1] (local), [F4] (pin_def). Move the flashing cursor to pin 10 with the arrow keys and press [F4] (ign/comp). Note that when pin 10 was ignored, the pin outline was no longer displayed.

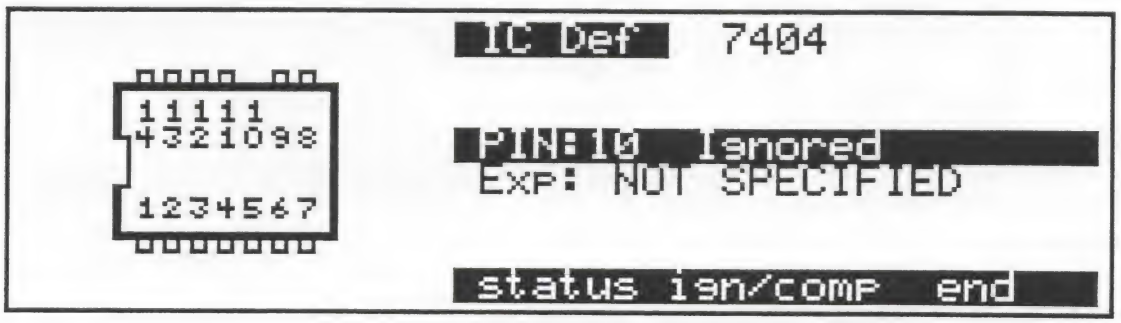



Figure 101

Press [F5] (end) to accept the change, and press [TEST] to test U25 again.

You may experiment will setting Condition Checks on various pins by going to Pin_Def again, positioning the cursor on a pin of interest and pressing F3 (status) repeatedly to define various attributes. F5 (end) must be pressed to save any changes when exiting this mode. In the screen below we have just defined pin 1 as "must be low", pin 2 as "must be high", pin 3 as "must be active" and pin 4 as "must have 1 MHz signal within 1 % tolerance".

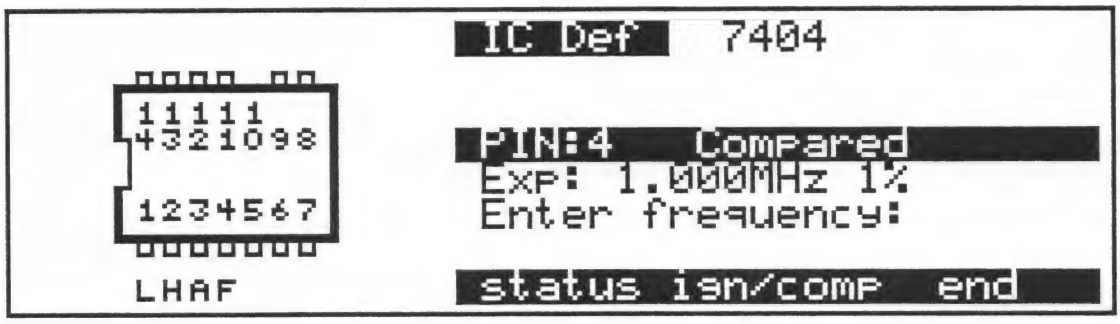



Figure 102

So far in this exercise we have tested all of U25 except pin 10. This pin may be tested if other pins are ignored.

Re-load the device library description for a 7404 from the manual level to restore all the parameters to their default values. This is the setting that has pin 10 failing. Find a Performance Envelope setting that allows this pin to pass. For example, try setting F_Mask to 100 ns and set Threshold to 1 V.

When testing U25 with this setting, pin 10 usually passes while other pins may fail. Use the Pin_Def parameter to ignore these other pins and obtain a PASS test result.

A third way to test U25, since we know how it is used in the circuit, is to ignore pin 10, while at the same time placing a conditions test of active (A) on pin 10. This test will allow the other gates of U25 to be tested with a limited F_Mask, and at the same time ensure that pin 10 is not "stuck" or shorted (after lowering the threshold to 1 volt, this pin will show as being active).

**Test Concept**

A single device may be tested twice, each time with different parameters, by ignoring pins using Pin_Def. In this way a high quality of test may be achieved for the entire device.

# 13 RD Test

*Reference Device Test or RD Test is a truth table verification of a device inserted in the ZIF socket. It is used to verify the presence of an RD when Simulation is not enabled.*

**Exercise 1**

Test an IC on the board after disabling RD Test.

From manual level load the device library description for a 7400, press (7), (4), (0), (0), (ENTER). If this device is simulated press (ETC), (F3) (rd).

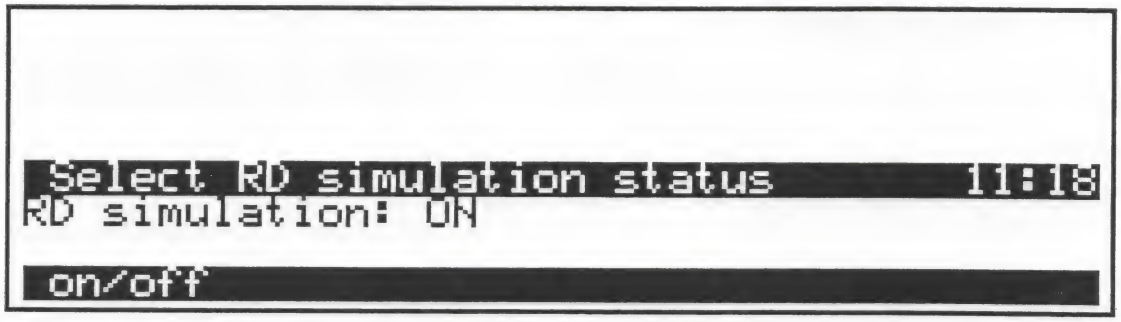



Figure 103

Disable simulation then by pressing (F4) (rd_sim), (F1) (on/off), (ENTER), (ESC). Clip on U42 (use U14 on the sales demo trainer), and press (TEST).

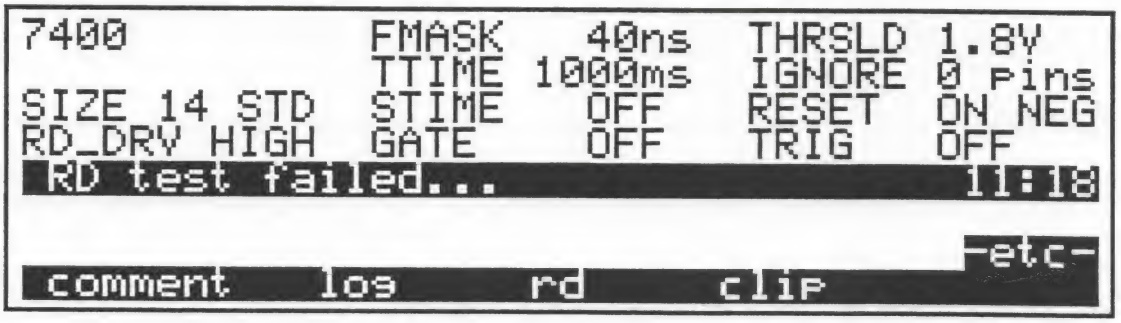



Figure 104

It is necessary to insert a 7400 Reference Device in the ZIF socket, since RD Test verifies that the RD is functioning correctly (according to a truth table) before proceeding with comparison testing. This truth table test should be thought of as a static test, since it is done at about 10 KHz data rates.

Instead of inserting a Reference Device, disable RD Test: press (F3) (rd), (F2) (rdt_off),

(ESC).

With the RD Test disabled, it is possible to "test" U42 without anything in the ZIF socket. In fact, you can clip on another 14 pin device like U10 (use U11 on the sales demo trainer), which is a 7474, and it will appear to pass as well (as long as no pins on the device are floating). This illustrates that when there is either no RD (actual or simulated), or an RD that is tri-state so that no pins are output pins at that moment, the DifTest circuit of the 900 will treat all pins as input pins, and no comparison testing will occur. For this reason, the RD Test should not be disabled unless there is a good reason to do so. As long as the RD Test is enabled, a check will be done to ensure that a correct RD is available for comparison.

This characteristic of the 900 is what enables "natural" Gating of the RD (see the description for the Gate parameter in this section).

You may re-enable RD Test using the same keys used to disable it.

**Exercise 2**

Create a RD Test for a PAL device.

From manual level load the device library description for a PAL22V10, press (P), (A), (L), (2), (2), (V), (1), (0), (ENTER). Insert the PAL labelled DEMO3 into the ZIF socket. Execute a generic RD Test pattern on this PAL by pressing (F3) (rd) and (F1) (rdt_run).

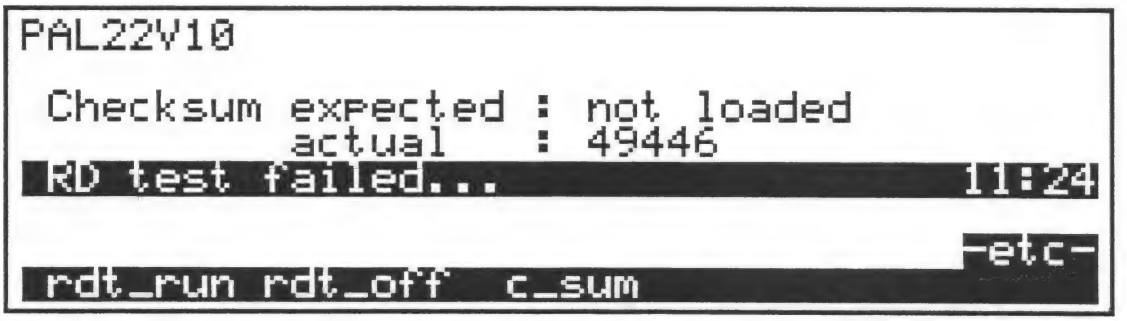



Figure 105

The characteristic response of the PAL is calculated as a checksum. Load this value by pressing (F3) (c_sum), typing in the actual number found (49446), and (ENTER). Now, when you press (F1) (rdt_run) to perform RD Test, you should obtain a passing result.

This same process is used to calculate a characteristic checksum for PROM and EPROM devices.

Press (ESC) to return to the manual menu, followed by (ETC).

**Test Concept**

RD Test performs a vital check that there is indeed a Reference Device inserted if required. There are three types of RD Test:

- Truth Table Pattern that is part of Library information.
- Checksum that is calculated from a standard pattern.
- Presence detection that a device of the expected size is in the ZIF socket.

Presence is used when an RD is unknown (e.g. testing with the Size parameter) or the RD cannot be functionally verified (e.g. DRAM).

# 14 RD Drive

*Reference Device Drive or RD Drive specifies whether an RD has the ability to drive 1 LS load (High setting) or is weaker (Low setting). This defines the load presented by the ZIF socket to the RD. RD Drive Low also limits the maximum comparable data rates to 12 MHz.*

The left side of the display shows "RD_DRV HIGH" by default (some older versions of Library firmware have a LOW default setting for some devices).

Some vendors of 27XXX series EPROMs have been found to supply devices that are weaker than 1 LS load drive. Such an EPROM will produce a different checksum for the RD drive High and Low settings, or indicate failed pins on the High setting. A 27XXX type device was not provided with this course, however, to verify an EPROM to see if it is weak and should have an RD drive Low setting when used as a RD place it in the socket and execute the RD Test to calculate a checksum for a 2764 you would press [2], [7], [6], [4], [ENTER], then [F3] (rd), [F1] (rdt_run).

Press [ETC], [F3] (rd_drv), [F1] (high/low), [ENTER] to change RD drive to Low.

Re-execute the RD Test to calculate a checksum: press [ETC], [F1] (rdt_run). If the checksums are different, the required RD Drive setting for this EPROM is Low. If they are the same, the setting should be High.

We have found that the RD_DRV low setting is needed with some EPROM and Static RAM devices. CMOS devices of the 4000/14000 families often have output drive capability too weak for even the RD_DRV Low setting, and may only be tested with a Simulated device.

**Test Concept**

Certain devices, such as some second-sourced EPROMs, are too weak to drive the normal comparison circuit through the ZIF socket. Such devices will appear the same as an empty socket to the 900, and we know from a previous exercise that this causes all DUT tests on a board to pass. RD Drive should be set to low for such weak devices. This may be determined by running RD Test at both High and Low settings of RD Drive.

# 15 Simulation

*Simulation permits Reference Devices to be simulated by a reconfigurable ASIC device in the 900. This takes the place of inserting an RD in the ZIF socket for common TTL and CMOS devices.*

The hardware Simulation of the 900 offers is not to be confused with software simulation of devices that is required with some other types of automated test equipment. The 900 always requires that a reference device is present in order for the comparison to take place, recall that the 900 does not stimulate the UUT. Therefore, it is ***not*** possible to "learn" the signals from a good board, store them, and call the stored signals back when testing another board. What ***may*** be stored for later use are the test parameters adjustments that were necessary to obtain a Pass test result on a good board.

**Exercise**

Test a DUT using an actual and simulated RD, and compare the Performance Envelope settings.

Ensure that the Cartridge for this course is inserted in the 900. Simulation Library files are resident on it for most of the devices found on both the self-paced trainer, and the sales demo trainer. If you attempt to load the library description for a 7400 without the Cartridge inserted, it appears on the display as a standard (unsimulated) device. The one exception being certain demonstrator 900s that have a few simulation patterns resident in them. Simulation Libraries may be downloaded from a PC to the 900 Cartridge or System RAM using the Library Utility software package.

From the manual menu level load the device library description for a 7400, press [7], [4], [0], [0], [ENTER]. Note that it is a simulated RD, and clip on U42 (use U14 on the sales demo trainer). Press [TEST]. Note that F_Mask is set to 30 ns (unless the global default is still changed to 40 ns from an earlier exercise), and the test is passing.

Change F_Mask to 20 ns and repeat the test, press [F1] (local), [F2] (f_mask) [2], [0], [ENTER], [TEST]. The FAIL test result is because F_Mask is not large enough to compensate for the performance difference between DUT and RD.

Simulated RDs usually require a minimum F_Mask setting of 30 or 40 ns.

Insert a 7400 Reference Device in the ZIF socket and disable Simulation. Press [ESC], (if you are still in a fail screen press [ESC] twice), then [ETC], [F3] (rd), [F4] (rd_sim), [F1] (on/off), [ENTER], [ESC].

Now retest U42 using the actual RD. It should pass, even with F_Mask set to 20 ns.

**Test Concept**

Simulation is a convenient way to automate the Reference Device handling. The F_Mask is typically 10 to 20 ns greater than if an actual RD were used. Since an F_Mask of 40 ns corresponds to a maximum signal speed of 12 MHz (and 30 ns/16 MHz, 20 ns/20 MHz), the user may want to use actual Reference Devices for high speed areas of a UUT.

# 16 Shadow

*The Shadow RAM feature solves initialization problems with RAM testing by permitting comparison testing only for those RAM address locations written into since the start of the test. The Shadow Pattern is a file similar to a Simulation Library that must reside on Cartridge or System RAM (it may be downloaded from a PC using the Library Utility package). However, unlike a Simulated device, a physical RAM chip is still required for testing.*

**Exercise**

Test a RAM with and without Shadow.

From manual level load the device library description for a 41256, press [4], [1], [2], [5], [6], [ENTER]. Place the 41256 Reference Device in the ZIF socket.

The RAM circuit on the self-paced trainer board was originally engineered right to the limit of a 41256's operating specifications. The RAS signal hold time *averaged* 20 ns on the boards that were examined. The databook minimum for this value is 15 ns. Because of the maximum potential ± 2 ns pin-to-pin signal skew of the 900, occasionally the databook minimum is not met for the RD, and failures result. This situation presents a very narrow window of voltage levels that will allow the 900 to test this device. Clip on U70 (use U90 on the sales demo trainer) and use the Learn feature to identify the correct Threshold and Fault Mask settings, press [F5] (learn), [F2] (execute). When a suitable pair of settings has been identified, press [F5] (end), and [ESC] to return to the manual menu. If a suggested pair of settings is not made due to insufficient Pass results, try changing Threshold to 2.0 Volts in the local menu (the sales demo trainer may be tested without the preceding adjustment). Press [TEST]. to run a the test with the Shadow feature enabled.

Notice that the test time of 1000 ms (and Reset) are used four times (Page 0 through Page 3). This is because the RAM Shadow is a 64 Kbyte high speed RAM that records all address locations written during the test. It overlays its 64 Kbyte space four times to cover the 256 Kbytes of this DUT.

An additional feature is the ability to examine how many locations were written during the test. Note that this information is presented just below the Status Line on the screen after each test involving the RAM Shadow.


Figure 106

You can experiment with changing the test time, or removing the RST patch lead to see the effect on the number of addresses written during the test. Note that when test time is set to continuous, pressing (NEXT) will advance the Page (0, 1, 2, 3) of Shadow overlay.

Disable the Shadow feature: Press (ETC), (F3) (rd), (F5) (shadow), (F1) (on/off), (ENTER), (ESC).

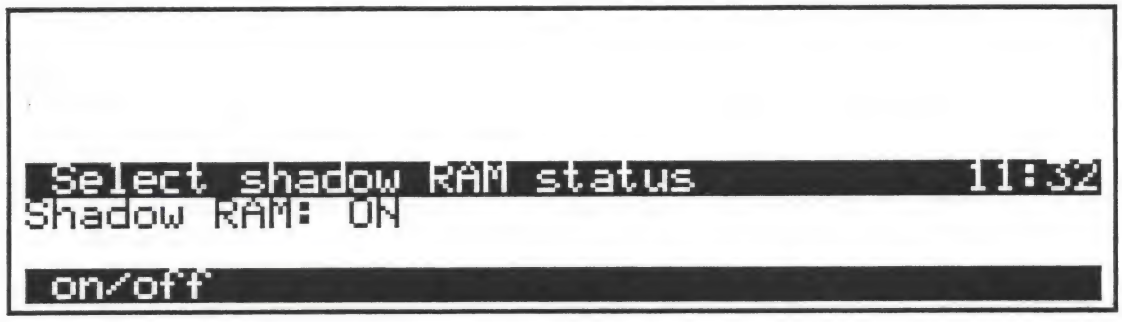



Figure 107

Test U70 again without the Shadow enabled, press (TEST).

The apparent failure is because the board activity immediately after reset performs a "read before write" of some RAM locations. The RD and the DUT therefore have different data in these locations and they fail comparison. This can be verified by setting Reset Offset to -100 ms to wait for the indeterminate activity to occur before comparison testing. A better solution is to enable Shadow, or to use a Trigger whenever testing RAM. Otherwise it is not known if any failures result from a bad device, or from an invalid comparison (comparison of data in the DUT with random information in the RD).

On occasion, the test will pass despite the "read before write" situation. This happens when, by coincidence, the data in the DUT and the data in the RD are the same. After a RAM device has been without power for a period of time, the data in the dynamic memory cells will tend to shift to a nominal state of either high or Low, depending on the design

of the device. Care must be taken when developing a test sequence that the conditions for proper initialiaztion of the DUT and RD are defined, or false failures may be recorded later due to different random data.

**Test Concept**

Shadow takes care of initialization problems which enable us to distinguish errors caused by UUT stimulus (Read before Write), or the failure mode of the board. In addition, the "Addresses Written" shown in the results screen is a good indicator of the quality of the RAM test stimulus.

# 17 Clip Check

*Clip Check verifies that logic 1 is on the Vcc pin and logic 0 is on the Ground pin of a device. This is used as an orientation check for the Clip, and to ensure that the clip is fully seated on the device.*

**Exercise**

Disable and re-enable Clip Check.

Load the library description for a 7400, press (7), (4), (0), (0), (ENTER). Place a 7400 in the socket if Simulation is not enabled. Clip over any 20 pin device on the board. Press (TEST).

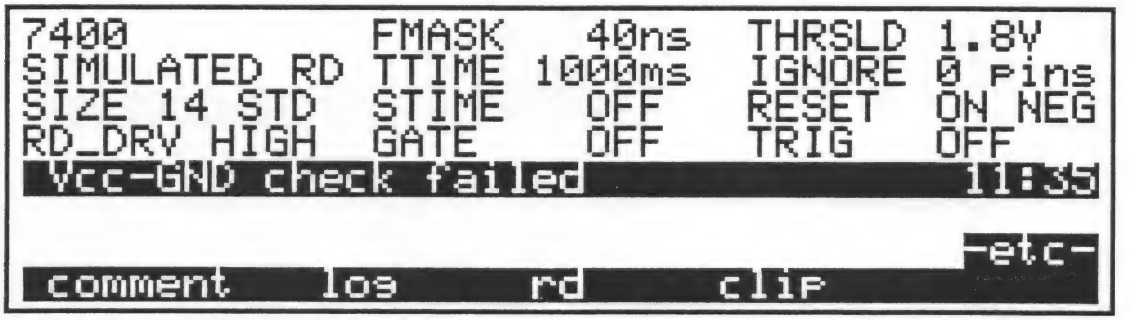



Figure 108

Note that the proper signals were not measured on the power and ground pins of the clip as indicated by the "Vcc-GND check failed" error.

Disable the clip check: Press (ETC), (F4) (clip), (F2) (clip_chk), (F1) (on/off), (ENTER), (ESC).

With the clip still over a 20 pin device, press (TEST). Note that the 900 does not indicate that the clip was not properly positioned this time.

**Test Concept**

Clip Check may be disabled to disregard the orientation of the Test Clip on a DUT. This can be useful when checking signal activity on devices larger than 28 pins.

# 18 Float Check

*As a default setting, Float Check automatically verifies that each pin of the DUT was driven during every test. This is a very simple and convenient way to locate open traces to the DUT, and may be disabled pin-by-pin, or for the whole device.*

**Exercise**

Load the device library description for a 7427, press [7], [4], [2], [7], [ENTER]. Insert a 7427 Reference Device in the ZIF socket if the device is not simulated. Clip U32 (use U81 on the sales demo trainer), and press [TEST]. The test should fail in a manner similar to what is shown below.


Figure 109

Turn to the description for a 74LS27 in the TTL Databook. Note that pins 1, 2, and 13 are all of the inputs for one gate of the device. This is a very strong indication that this gate is not used by this circuit design. The float test will fail unused input pins and gates. Usually, once those unused pins and gates have been accounted for (by disabling the float check – see below) during test sequence development on a known good board, any failures result from open traces or bad components.

By consulting a good data databook during test sequence development, most boards can be tested thoroughly - even if schematic diagrams are not available for that board. This same principle applies when testing in immediate mode on a failed board, though care must be taken that the actual failure is not compensated for by adjustments to the test parameters.

To disable testing of this gate, press [ESC], [ETC], [F4] (clip), and [F1] (float). Position the cursor by the "Z" character located at pins 1, 2, and 13. At each pin location press [F3] (status) to remove the "Z" character, and thus disable the Float Check for those pins.

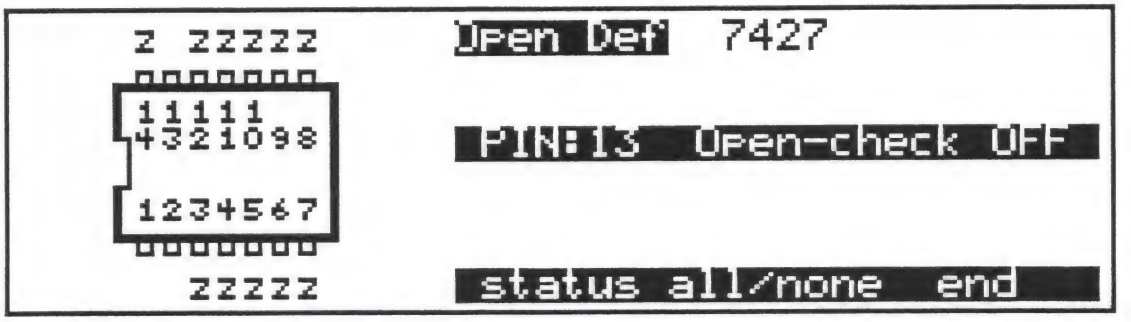



Figure 110

When all three have been disabled press (F5) (end) to store the changes. Press (ESC), (TEST) to run the test again.

**Test Concept**

The float check detects open traces to input pins that would otherwise require substantial troubleshooting time and effort to detect. The float check also alerts the 900 operator to conditions on the board, such as poor clip contact and unused pins and gates, that could otherwise cause inconsistent test results.

# SECTION 5
## Library Development

## 1 Device Libraries

*In this section you will create two new device library descriptions. The file that contains the commands for these entries will be created using the keyboard of the 900, though it could just as readily be created on a Personal Computer using any ASCII word processor, and downloaded to the 900.*

*Unlike Simulation library entries, standard library entries may be created by anyone. A standard library entry contains such information as truth table data, and synchronization requirements. Standard library entries always require a physical RD be used with them.*

## 2 Library Syntax Rules

When creating Library files there are four basic rules that must be followed.

- The first column is reserved for Labels, and must be empty in a library file.
- There must be at least one space separating parameters.
- A command will only be recognized once per complete entry (if you have two lines that use the same command in a single entry, only the last will be recognized).
- Each complete entry must end with a colon.

To make the entry more readable extra tabs and spaces are recommend. Examples will be shown with extra tabs and spaces.

In order to create a new library entry for a device you must identify how much information is available to you about the chip and you must decide how thorough of an entry you need.

# 3 Editing Library Files

This exercise will write a library file containing entries for a 7400 and 7474 device. By entering the following keystrokes starting at the 900 power-up screen, a new library file named "LIB1" will be created and opened.

Either insert the RAM cartridge that came with your 900 (the training cartridge is actually a ROM cartridge), or substitute F5 (:SYST) for F4 (:CART) in the following command. Press F3 (develop), F3 (rd_lib), F4 (edit), F2 (into), L, I, B, 1, F3 (.type), F2 (.LIB), F4 (:CART), ENTER.

Note: Pressing F2 (into) is used to create a new file, if the file already existed, the function key F2 (into) would not be pressed).

The file should be open now. Since it is a new file the Top and Bottom markers of the file will both be on the screen, with nothing between them. Because it is simpler, we will create the entry for the 7400 chip first. Chapter 7 of the 900 Operator Manual describes the possible commands for a Library file, along with several examples. Appendix II of the 900 Operator Manual describes each command separately, with syntax notes and examples.

# 4 Device Definition

A library entry can be as simple as two lines, or very complex and thorough. The bare minimum that must be in an entry is a name for the new chip, how many pins it has, and where power and ground are located. Below is an example of the shortest possible library entry.

```
NAME    7400
SIZE    14:
```

In the above entry, since power and ground are in the "standard" locations, (e.g. Vcc = [pin count], Gnd = [pin count divided by two] they are not specified).

For any entry in a Library file, a name must be given. This name will become the "permanent" library name for this device. Usually, the manufacturer's code (i.e. 7400) is used, however any name can be used. Be sure that the name makes sense for your application or you will have to make a list of chips in your library, and what they were called.

One example of a non-standard name for a chip might be a PAL device that has been programmed for use on a particular board, and has a label affixed to the chip. If the label reads "DEMO3", it would make sense for the Library entry to have the same name, since the technician will only be able to read the label on the chip, not the manufacturers codes. In this example we will use the manufacturer's codes for both devices. The name is entered as shown below. Note that the line begins one tab away from the margin, one space is adequate - but the tab makes for easier reading. There must also be at least a single space between the NAME command and the actual name. Tabs were used for separation below.

```
NAME    7400
```

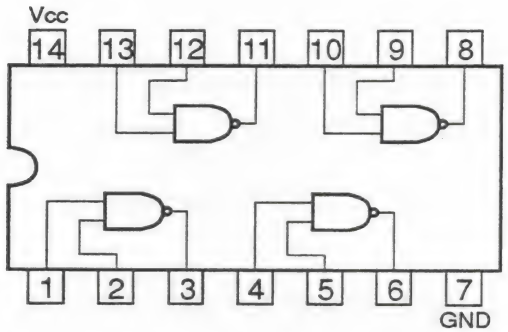
The SIZE command must be second (when the SIZE command is issued, many of the other test parameters are returned to their default settings). This tells the 900 how many pins on the test clip will be used, and also which pins of the reference device socket must have power and ground applied to them. For chips that have "standard" power and ground configurations, in this case power on 14 and ground on 7, the 900 defaults to the correct settings.

```
NAME    7400
SIZE    14
```

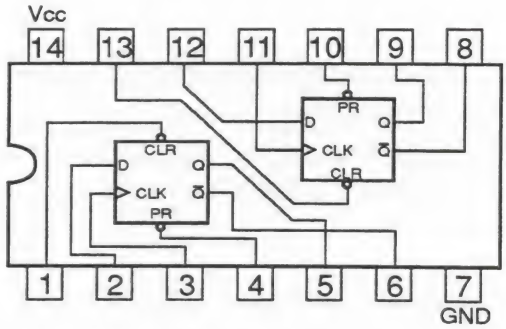
# 5 RD Test

To continue, we need information that is readily available from an IC databook, such as the one provided with this course. Examine the TTL Databook descriptions for a 74LS00 and a 74LS74 device. Below is excerpted the logic diagram and truth-table from the information found on these two chips.

Using information collected from the databook, a Reference Device test can be written. The truth table shown under the drawing of the 7400 chip below indicates the responses for any one of the four gates in the 7400.




74LS00




74LS74

Truth Table:

| Input 1 | Input 2 | Output |
|---|---|---|
| H | H | L |
| L | H | H |
| H | L | H |
| L | L | H |

Truth Table:

| CLR | PR | D | Q | $\overline{Q}$ |
|---|---|---|---|---|
| L | L | X | H | H |
| L | H | X | L | H |
| H | L | X | H | L |
| H | H | *h | H | L |
| H | H | *l | L | H |

* indicates state of referenced input prior to the LOW to HIGH clock transition.

Figure 111

The RDTEST VECTORS command has several qualifiers that can be given with it. We will use the command without a qualifier, indicating that we will provide test vectors for the 900 to use to verify the chip in the reference device socket. Each column corresponds to a pin of the chip, and spaces are ignored. Each row corresponds to one set of vectors and expected responses for the whole chip.

Pin1 Pin2 Pin3 Pin4 Pin5 etc.

Vector set 1
Vector set 2
Vector set 3
etc.

Examining the chip drawing above, we learn that pins one and two are input pins, and pin three is an output put. From the truth table we learn that if pins one and two are both high, (logic 1), then output pin three will be low (logic 0). The Vector list for these first three pins is shown below, using the proper syntax that is described in Appendix II of the 900 Operator Manual.

```
NAME      7400
SIZE      14
RDTEST    VECTORS
11L
```

The truth table for all possible functions of the chip are shown below. For illustration, all extra spacing has been removed. This is the minimum spacing permitted (one space from the margin, and one space between parameters). Also, all four gates were tested simultaneously, rather than one at a time while holding the remaining three unchanged.

```
NAME 7400
SIZE 14
RDTEST VECTORS
11L11LLL11L11H
01H01HLH01H01H
10H10HLH10H10H
00H00HLH00H00H
END_VECTORS:
```

It should be evident that on a large entry it can become very difficult to read the listing if spaces are not inserted. To make this easier to read in subsequent listings, each separate gate will be isolated by inserting spaces between each set of pins and the power and ground pins.

Note that according to the definitions listed in Appendix II for the VECTORS argument, inputs are shown with "1" or "0", and outputs (and power and ground) are shown with "H" or "L". This distinction is made so that the 900 will know which pins should be stimulated, and which pins should be measured.

Since a 7400 chip is categorized as a combinatorial device (in all cases outputs can be determined simply by looking at the input values - no clock or combination of inputs are

necessary to produce the expected output), this is all that is necessary for a Library entry. Entries are terminated with a colon. If a colon is not placed at the end of an entry, the 900 will continue to read successive lines of the file until a colon is encountered. Whatever the last commands read were is what will be loaded for test execution. The complete entry is as follows.

```
NAME        7400
SIZE        14
RDTEST      VECTORS
11L  11L  L L11  L11  H
01H  01H  L H01  H01  H
10H  10H  L H10  H10  H
00H  00H  L H00  H00  H
END_VECTORS:
```

Repeating the process described for the 7400, below is listed the entry for a 7474 including the RDTEST vector table. This time we have written the vector list in such a way that only one of the two halves of the chip is exercised at a time, while the other is held in a static state. An explanation of what action is being done by each vector line is given on the far right.

```
NAME        7474
SIZE        14
RDTEST      VECTORS
0000HH  L  HH0000  H      ; chip (both halves) forced to known states
0001LH  L  HH0000  H      ; only control line "clear" is asserted
1000HL  L  HH0000  H      ; only control line "pre-set" is asserted
1001HL  L  HH0000  H      ; controls removed, data input set low
1011LH  L  HH0000  H      ; clock line brought hi to cause rising edge
1101LH  L  HH0000  H      ; data input set hi, clock set low
1111HL  L  HH0000  H      ; clock line brought hi to cause rising edge
0000HH  L  HL0001  H      ; (above cycle repeated for other half of chip)
0000HH  L  LH1000  H
0000HH  L  LH1001  H
0000HH  L  HL1101  H
0000HH  L  HL1011  H
0000HH  L  LH1111  H
END_VECTORS:
```

Although more than one input was changed on a single line of vectors, normally this is not done. It was not a problem with this chip since it latches data only on a clock edge, and the clock was toggled without altering any inputs at the same time. Inputs are usually changed one at a time to avoid the possibly of creating a race condition on the reference device.

# 6 RD Synchronization

Unlike the 7400 chip, the 7474 is categorized as a synchronous device. The 7474 has outputs that are not completely dependent upon the inputs. As indicated by the truth-table, the clear, pre-set, and clock lines, together with the data input line will determine the value of the outputs. A good general rule for determining whether a chip is combinatorial or synchronous, is to ask the question "is the data latched by the chip in any way?" If the answer is yes, then the chip in question is probably a synchronous chip. The reason that this is important, is that the 900 must be informed at some point (either in the library entry or in the .LOC file) that synchronization of the RD chip and the DUT chip is necessary, otherwise false comparison failures will result.

In this case it is fairly easy to explain to the 900 what would constitute a state of synchronization between the two chips. By examining the databook information we learn that:

- If the control line "clear" is asserted, the chip will latch (and thus output) a known state.
- If the control line "pre-set" is asserted, the chip will latch a known state.
- If a rising edge is observed on the clock line, the chip will latch the input data

By taking the above synchronization information, we can quickly write a set of synchronization commands that inform the 900 of these three possibilities. Referring to the definition in chapter 7, and the explanation of command syntax in Appendix II of the 900 Operator Manual, we find three commands that will be necessary; sync_cond, sync_vect, and sync_pins.

The first command, sync_cond, defines for the 900 what conditions to watch for that would mean that both chips (DUT and RD), have been brought to the same latched output states. The 900 will devote approximately three fourths of the value of the parameter s_time to watching for these conditions to occur. The command is written as follows for one half of the chip, inserting the information identified above.

SYNC_COND < 1 P1=L + P4=L + P3=R >

The command is then read as follows, left to right: one occurrence of the expression within the brackets, first condition is if pin 1 (clear) goes low, (or) second condition is if pin 4 (pre-set) goes low, (or) third condition is if a rising edge is observed on pin 3 (clock). By using the "+" symbol for "or", we tell the 900 that any one of these conditions is sufficient to cause synchronization. The whole sync_cond command line is then:

SYNC_COND < 1 P1=L + P4=L + P3=R > * < 1 P10=L + P13=L + P11=R >

Since there are two identical halves of the chip, the command line now shows the

conditions necessary for both halves. Along with the necessary conditions there is the "*" symbol which indicates that any one of the conditions from the first group must happen, ***and*** any one of the conditions for the second half.

After the 900 has waited the specified amount of time for synchronization to occur as a result of activity present on the circuit board, and synchronization has not yet happened, the remaining time will be used attempting to force the reference device present in the socket of the 900 to "catch-up" to the state of the device on the board. This is when the command sync_vect is used. Similar to the rdtest vectors list, the sync_vect list is used by the 900 to stimulate the chip in the 900 socket. With this chip, the 7474, the simplest method for forcing one chip to the same state as the other, would be to load one with the same data that the other has loaded. In this example, if the data value measured on the "Q" output of the chip on the board were placed on the "D" input of the chip in the socket, and the chip in the socket clocked, they would then have the same data latched in each. By achieving synchronization in this manner, we allow for the data to be any combination of values for the two halves of the chip. This means that the sync_vect list will be simpler too. For the first half of the chip this is expressed as follows:

SYNC_VECT 1 < 1 H P3=C P2=D5 >

The command is then read as follows, left to right: (outside the bracket) one repetition of the entire line of expression, (inside the bracket) one repetition of the contents of this set of brackets, any pin not specifically identified should be made high during execution of this bracket, pin 3 is clocked, while the data found on pin 5 of the chip on the board is placed on pin 2 of the chip in the socket. The expression for the whole chip is:

SYNC_VECT 1 < 1 H P3=C P2=D5 P11=C P12=D9 >

As you may have noticed, the order in which each pin parameter appears is not important, as long as syntax requirements are met. The 900 will sort out the order. In the above example the vector list is simple enough to remain on one line. If any command exceeds the maximum line length of 254 characters it may be continued on the next line by using the @ symbol as a line terminator for the previous line. The first column is still reserved for Labels, and may not contain any characters from the command.

The last command that the 900 needs for synchronizing this chip is the sync_pins command. Sync_pins specifies the pins of the chip on the board which should be inactive during the time that synchronization vectors are being applied to the chip in the socket. While synchronization vectors are being applied to the chip, the 900 will check for synchronization after each line. If the two chips are found to be in synchronization after a vector is applied, any remaining s_time will be discarded and the comparison test will begin. After all synchronization vectors have been used, the 900 will look to see if there had been any activity on the pins identified by the sync_pins command. If activity on

these pins was observed during the time sync vectors were being applied, and there is still s_time remaining, then the 900 will start the sync_vect list over again. If there had been no activity, and the two parts are still not in synchronization, the 900 will fail the synchronization - assuming that a bad device is present. For this reason, it is important to provide a set of vectors that exercise all gates in the device. Below, for this command we simply list the pins that can affect the output data. In this case they will be; clear, pre-set, and clock (for both halves).

```
SYNC_PINS      1 3 4 10 11 13
```

This is all that is necessary for a library entry for a 7474.

# 7 File Compilation

The complete library file at this time is shown below. Note that the full entry for each chip ends with a colon.

```
NAME        7400
SIZE        14
RDTEST      VECTORS
11L  11L  L L11  L11  H
01H  01H  L H01  H01  H
10H  10H  L H10  H10  H
00H  00H  L H00  H00  H
END_VECTORS:

NAME        7474
SIZE        14
RDTEST      VECTORS
0000HH  L  HH0000  H
0001LH  L  HH0000  H
1000HL  L  HH0000  H
1001HL  L  HH0000  H
1011LH  L  HH0000  H
1101LH  L  HH0000  H
1111HL  L  HH0000  H
0000HH  L  HL1000  H
0000HH  L  LH0001  H
0000HH  L  LH1001  H
0000HH  L  HL1101  H
0000HH  L  HL1011  H
0000HH  L  LH1111  H
END_VECTORS
SYNC_COND   < 1 P1=L + P4=L + P3=R > * < 1 P10=L + P13=L + P11=R >
SYNC_VECT    1 < 1  H  P3=C  P2=D5  P11=C  P12=D9 >
SYNC_PINS    1  3  4  10  11  13
SYNC_GR_END:
```

As noted at the beginning, an entry can be as simple or as complete as desired. For the 7474 entry, you may decide that you have confidence in your reference chips, and therefore do not wish to create the rdtest vectors list. It is entirely up to you as to how much effort you wish to put into any one library entry.

Now that the two entries are complete, the file must be stored and compiled. This is done as follows: Press F5 (end), F3 (compile), L, I, B, 1, F3 (.type), F2 (.LIB), F4

(:CART), ENTER.

Assuming that there were no syntax problems encountered, the compiler will make two passes before returning a message that the compile process is complete. Be sure that you compile the file again each time it is edited, or the edits will not be included when the entry is called for during test execution.

The new entries may now be called from the Manual mode, Develop mode, and the RD Library mode in the same manner as other device library descriptions are called up. According to the order of precedence that the 900 uses in searching for requested library entries, the new entries will be selected before the entries having the same name in the firmware (ROM) library, (cartridge first, then system ram, and last system ROM).

When a library entry is requested the 900 will check all library files on the data cartridge for the requested entry. If that is unsuccessful it will check all library files in system RAM memory. As a last resort it will check the firmware (ROM) library. If it still can not find an entry with the requested name, it will report the following message, "Chip not found", accompanied by an error tone.

Refer to Section 7 of the 900 Operator Manual for additional information about device libraries.

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## D



## E



## F

## G



## I



## J



## L



## M



## O

## P



## R



## S

## T



## U

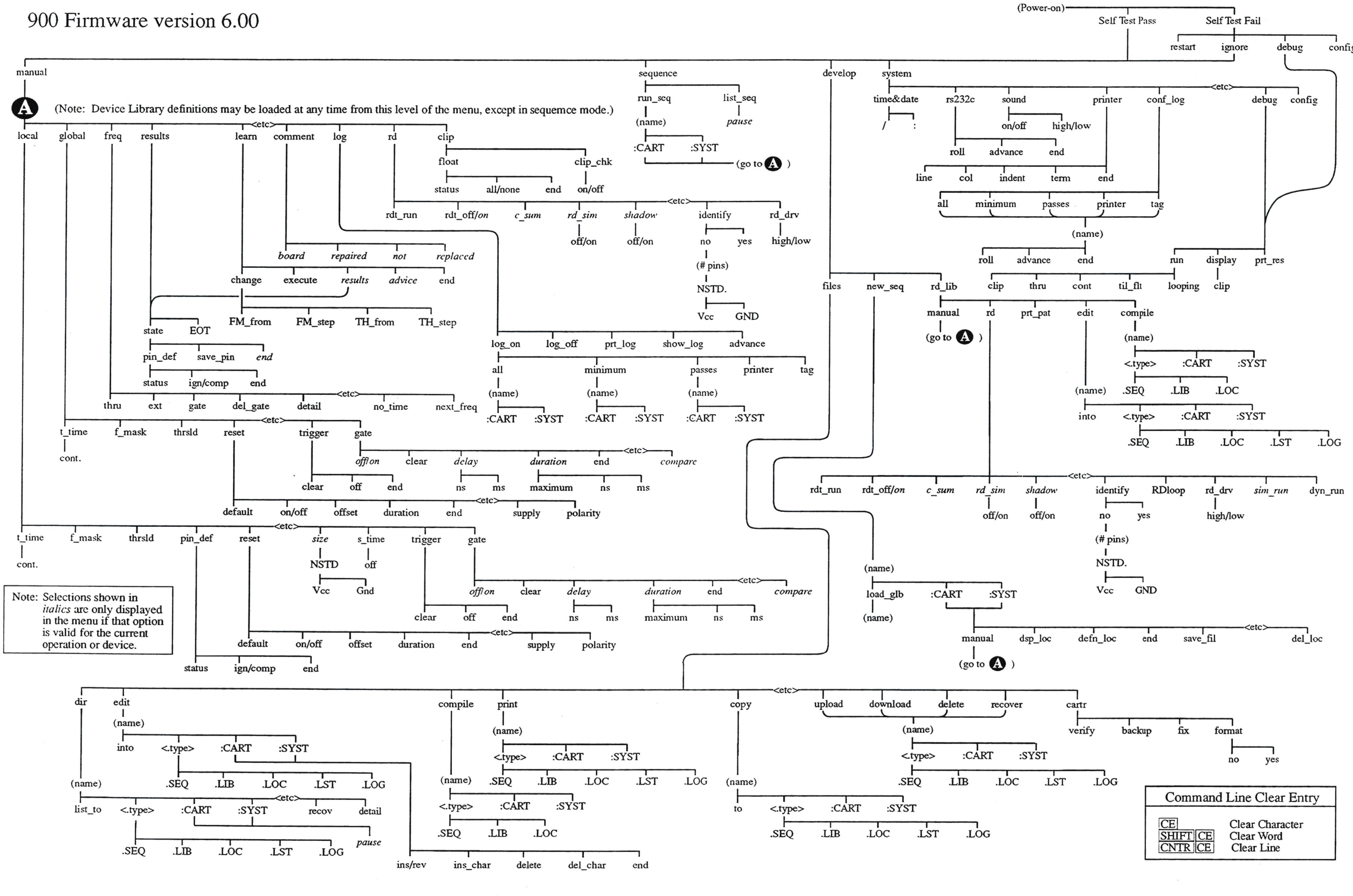


## V



## Z

# 900 Firmware version 6.00



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